



H55H-LD

Rev : 1.0

ECS CONFIDENTIAL

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13	PCH USB&PCIE&DMI
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REVISION HISTORY:


Rev	Date	Notes
V.A	2009/09/31	Initial version
V.0.1	2009/11/24	
V.1.0	2010/01/29	

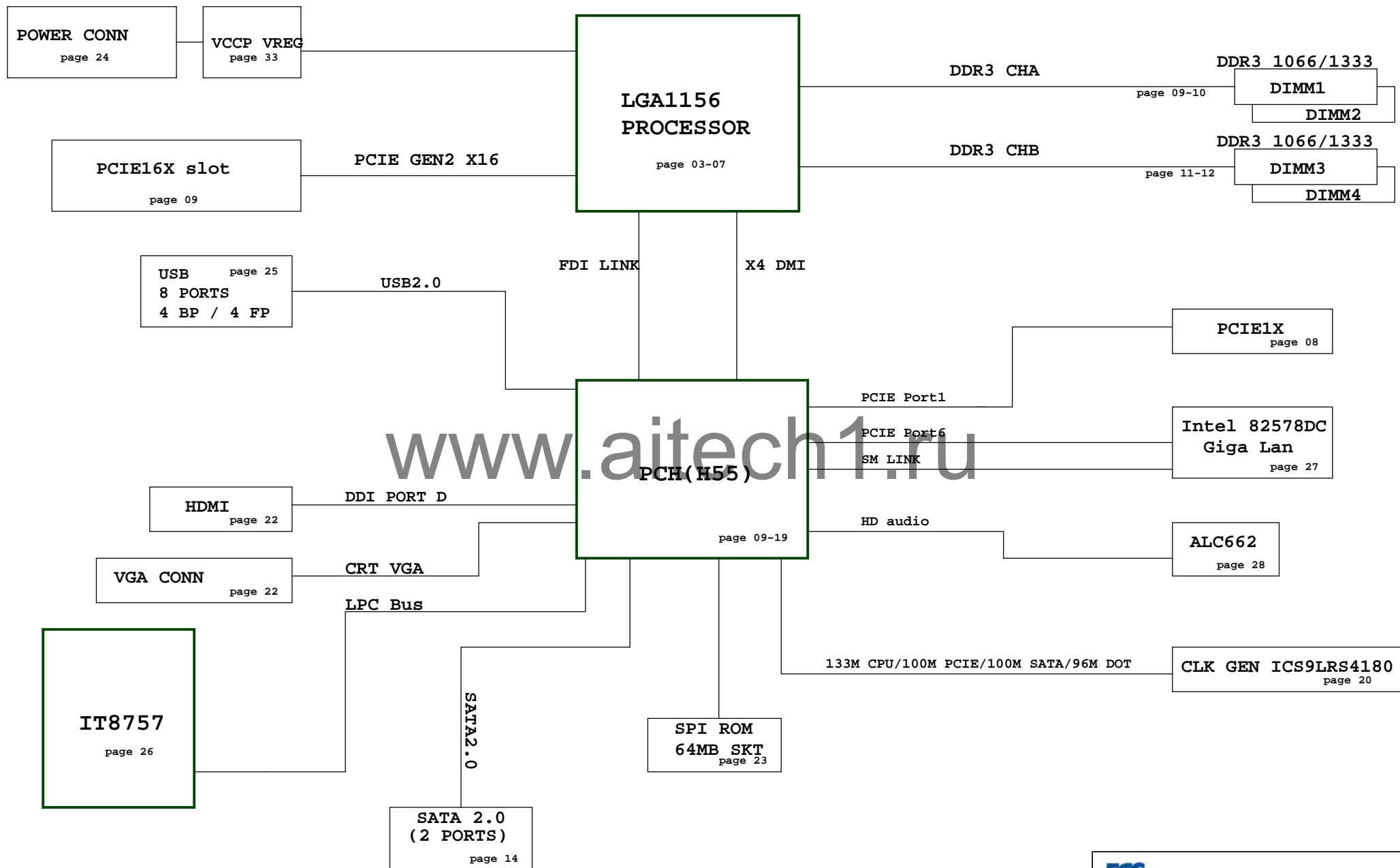
www.aitech1.ru

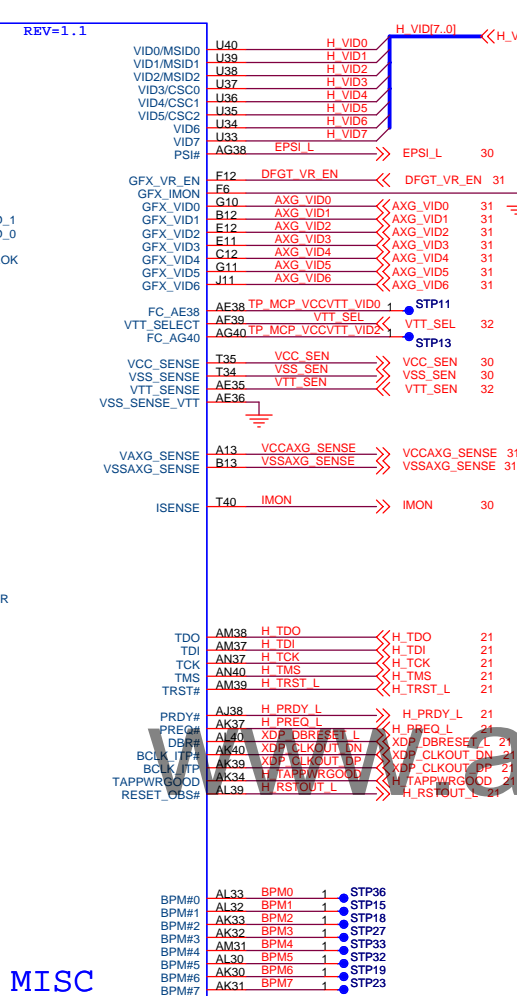
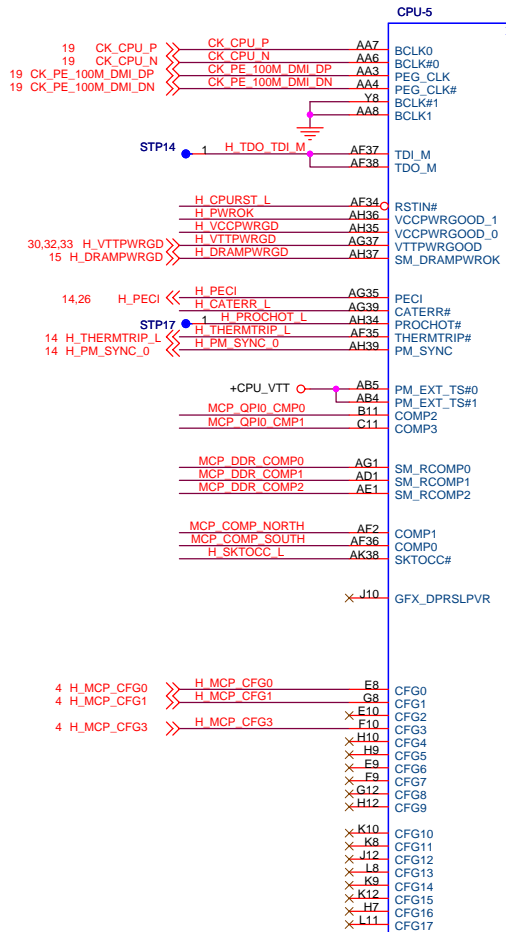
Note:

Design guide:

376563_376563_Piketon_Kings_Creek_Foxhollow_Platform_Design_Guide_Rev1_5

		Elitegroup Computer Systems	
File			
Cover Page			
Size	Document Number	Rev	
Custom	H55H-LD	1.0	
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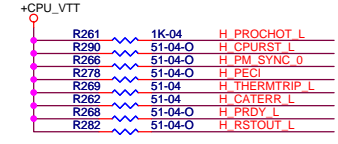
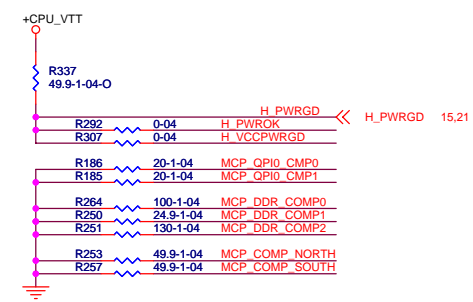




MISC

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LGA1156



Pipe A

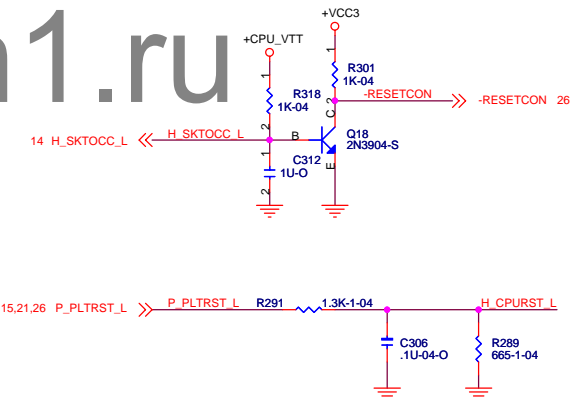
Pipe B

DISPLAY LINK


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LGA1156

BCLK(133MHz) for CPU/MEM/GPU
PEG_CLK(100MHz) for PCIE/DMI/FDI



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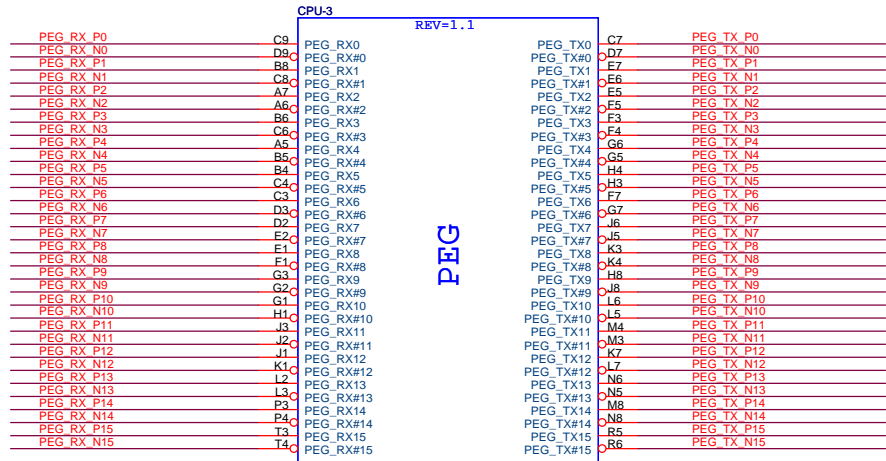
**Elitegroup Computer Systems**

File **CPU MISC&Flexible Display Interface**

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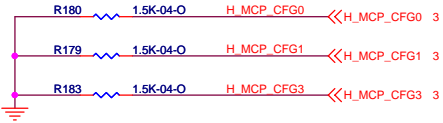
8 PEG_RX_P[0..15] >>>
8 PEG_RX_N[0..15] >>>
8 PEG_TX_P[0..15] <<<
8 PEG_TX_N[0..15] <<<



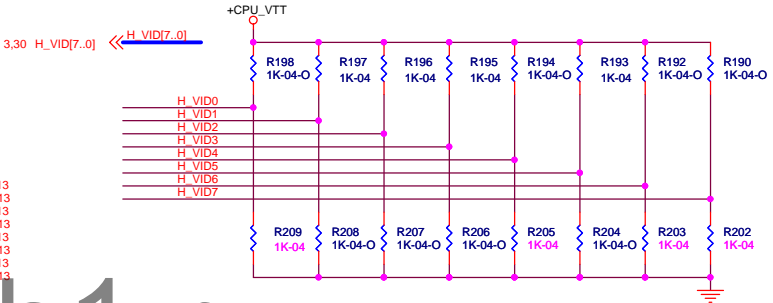
13 DMI.IT_MR_0_DP >>> DMI.IT_MR_0_DP
13 DMI.IT_MR_0_DN >>> DMI.IT_MR_0_DN
13 DMI.IT_MR_1_DP >>> DMI.IT_MR_1_DP
13 DMI.IT_MR_1_DN >>> DMI.IT_MR_1_DN
13 DMI.IT_MR_2_DP >>> DMI.IT_MR_2_DP
13 DMI.IT_MR_2_DN >>> DMI.IT_MR_2_DN
13 DMI.IT_MR_3_DP >>> DMI.IT_MR_3_DP
13 DMI.IT_MR_3_DN >>> DMI.IT_MR_3_DN

DMI_RX0 DMI_RX#0 DMI_RX1 DMI_RX#1 DMI_RX2 DMI_RX#2 DMI_RX3 DMI_RX#3
DMI_TX0 DMI_TX#0 DMI_TX1 DMI_TX#1 DMI_TX2 DMI_TX#2 DMI_TX3 DMI_TX#3

DMI_MT_IR_0_DP DMI_MT_IR_0_DN DMI_MT_IR_1_DP DMI_MT_IR_1_DN DMI_MT_IR_2_DP DMI_MT_IR_2_DN DMI_MT_IR_3_DP DMI_MT_IR_3_DN



CFG	Desktop Lynnfield						
0	1	11=1*16X	0	10=2*8X	1	0	Reserved
1	1		1		0	0	
	Clarkdale PCI Express Static Lane Numbering Reversal				Lynnfield		
3	0	Reversal			Reserved		
	1	No Reversal					
0,1,3 HAVE INTERNAL PULL-UPS							



POWER ON CONFIGURATION (POC) TABLE

	FUNCTION	Setting	Havendale	Lynnfield
VID0	MIS0	0	Support	Support
VID1	MIS1	1		
VID2	MIS2	1		
VID3	IMON CONFIG0	1	Icc(MAX)=110A	Icc(MAX)=110A
VID4	IMON CONFIG1	0		
VID5	IMON CONFIG2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

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CPU-1

REV=1.1

M MAA A0	AW18	SA_MA[0]	SA_DQ50	AK3	M DQS A DP0
M MAA A1	AW15	SA_MA[1]	SA_DQ50#0	AK3	M DQS A DN0
M MAA A2	AW15	SA_MA[2]	SA_DM0	AK2	M DQM A0
M MAA A3	AW15	SA_MA[3]	SA_D00	AH1	M DATA A0
M MAA A4	AW14	SA_MA[4]	SA_D01	AJ4	M DATA A1
M MAA A5	AW13	SA_MA[5]	SA_D02	AL2	M DATA A2
M MAA A6	AW14	SA_MA[6]	SA_D03	AL1	M DATA A3
M MAA A7	AW14	SA_MA[7]	SA_D04	AG2	M DATA A4
M MAA A8	AW12	SA_MA[8]	SA_D05	AH2	M DATA A5
M MAA A9	AT19	SA_MA[9]	SA_D06	AK1	M DATA A6
M MAA A10	AT19	SA_MA[10]	SA_D07	AK2	M DATA A7
M MAA A11	AW11	SA_MA[11]	SA_DQ51	AP2	M DQS A DP1
M MAA A12	AW11	SA_MA[12]	SA_DQ51#0	AP3	M DQS A DN1
M MAA A13	AU24	SA_MA[13]	SA_DM1	AN1	M DQM A1
M MAA A14	AT11	SA_MA[14]	SA_D08	AN3	M DATA A8
M MAA A15	AR10	SA_MA[15]	SA_D09	AN2	M DATA A9
M WE A L	AT22	SA_WE#	SA_DQ10	AR2	M DATA A10
M CAS A L	AU22	SA_CAS#	SA_DQ11	AM3	M DATA A11
M_RAS A L	AT22	SA_RAS#	SA_DQ12	AM2	M DATA A12
M SBS A0	AV20	SA_BS[0]	SA_DQ13	AP1	M DATA A13
M SBS A1	AU19	SA_BS[1]	SA_DQ14	AR4	M DATA A14
M SBS A2	AU12	SA_BS[2]	SA_DQ15	AR4	M DATA A15
M SCS A N0	AV21	SA_CS#0	SA_DQ52	AU4	M DQS A DP2
M SCS A N1	AW24	SA_CS#1	SA_DQ52#0	AU3	M DQS A DN2
M SCS A N2	AU21	SA_CS#2	SA_DM2	AU1	M DQM A2
M SCS A N3	AU23	SA_CS#3	SA_DQ16	AT4	M DATA A16
M SCKE A0	AU10	SA_CKE[0]	SA_DQ17	AU2	M DATA A17
M SCKE A1	AW10	SA_CKE[1]	SA_DQ18	AW3	M DATA A18
M SCKE A2	AV10	SA_CKE[2]	SA_DQ19	AW4	M DATA A19
M SCKE A3	AV10	SA_CKE[3]	SA_DQ20	AT3	M DATA A20
M ODT A0	AV23	SA_ODT[0]	SA_DQ21	AT2	M DATA A21
M ODT A1	AV24	SA_ODT[1]	SA_DQ22	AV4	M DATA A22
M ODT A2	AW23	SA_ODT[2]	SA_DQ23	AV4	M DATA A23
M ODT A3	AV24	SA_ODT[3]	SA_DQ53	AY6	M DQS B DP3
CK M DDR0 A DP	AR22	SA_CK[0]	SA_DQ53#0	AW6	M DQS B DN3
CK M DDR0 A DN	AR22	SA_CK[0]	SA_DM3	AV6	M DQM A3
CK M DDR1 A DP	AP18	SA_CK[1]	SA_DQ24	AW5	M DATA A24
CK M DDR1 A DN	AN18	SA_CK[1]	SA_DQ25	AY5	M DATA A25
CK M DDR2 A DP	AN21	SA_CK[2]	SA_DQ26	AU8	M DATA A26
CK M DDR2 A DN	AP19	SA_CK[2]	SA_DQ27	AY8	M DATA A27
CK M DDR3 A DP	AN19	SA_CK[3]	SA_DQ28	AU5	M DATA A28
CK M DDR3 A DN	AN19	SA_CK[3]	SA_DQ29	AV5	M DATA A29
DDR3_DRAMRST_L	AV8	SM_DRAMRST#	SA_DQ30	AV7	M DATA A30
STP25	AK22	SA_CS#4	SA_DQ31	AW7	M DATA A31
STP29	AK22	SA_CS#4	SA_DQ54	AR28	M DQS B DP4
STP30	AL23	SA_CS#5	SA_DQ54#0	AT28	M DQS B DN4
STP21	AK23	SA_CS#6	SA_DM4	AN29	M DQM A4
SA_DQ32	AN27	M DATA A32	SA_DQ32	AN27	M DATA A32
SA_DQ33	AT28	M DATA A33	SA_DQ33	AP28	M DATA A34
SA_DQ34	AP30	M DATA A35	SA_DQ34	AP30	M DATA A35
SA_DQ35	AN26	M DATA A36	SA_DQ35	AN26	M DATA A36
SA_DQ36	AR27	M DATA A37	SA_DQ36	AR27	M DATA A37
SA_DQ37	AR29	M DATA A38	SA_DQ37	AR29	M DATA A38
SA_DQ38	AN30	M DATA A39	SA_DQ38	AN30	M DATA A39
SA_DQ39	AV32	M DQS B DP5	SA_DQ39	AV32	M DQS B DP5
SA_DQ55	AW32	M DQS B DN5	SA_DQ55	AW32	M DQS B DN5
SA_DQ56	AW31	M DQM A5	SA_DM5	AW31	M DQM A5
SA_DQ40	AU30	M DATA A40	SA_DQ40	AU30	M DATA A40
SA_DQ41	AU31	M DATA A41	SA_DQ41	AU31	M DATA A41
SA_DQ42	AV33	M DATA A42	SA_DQ42	AV33	M DATA A42
SA_DQ43	AU34	M DATA A43	SA_DQ43	AU34	M DATA A43
SA_DQ44	AV30	M DATA A44	SA_DQ44	AV30	M DATA A44
SA_DQ45	AU33	M DATA A45	SA_DQ45	AU33	M DATA A45
SA_DQ46	AW33	M DATA A46	SA_DQ46	AW33	M DATA A46
SA_DQ47	AW33	M DATA A47	SA_DQ47	AW33	M DATA A47
SA_DQ56	AW36	M DQS B DP6	SA_DQ56	AW36	M DQS B DP6
SA_DQ57	AW35	M DQS B DN6	SA_DQ57	AW35	M DQS B DN6
SA_DQ58	AU35	M DQM A6	SA_DM6	AU35	M DQM A6
SA_DQ48	AW35	M DATA A48	SA_DQ48	AW35	M DATA A48
SA_DQ49	AY35	M DATA A49	SA_DQ49	AY35	M DATA A49
SA_DQ50	AV37	M DATA A50	SA_DQ50	AV37	M DATA A50
SA_DQ51	AU37	M DATA A51	SA_DQ51	AU37	M DATA A51
SA_DQ52	AY34	M DATA A52	SA_DQ52	AY34	M DATA A52
SA_DQ53	AW34	M DATA A53	SA_DQ53	AW34	M DATA A53
SA_DQ54	AV36	M DATA A54	SA_DQ54	AV36	M DATA A54
SA_DQ55	AW37	M DATA A55	SA_DQ55	AW37	M DATA A55
SA_DQ57	AR39	M DQS B DP7	SA_DQ57	AR39	M DQS B DP7
SA_DQ58	AR38	M DQS B DN7	SA_DQ58	AR38	M DQS B DN7
SA_DQ59	AT38	M DQM A7	SA_DM7	AT38	M DQM A7
SA_DQ56	AT39	M DATA A56	SA_DQ56	AT39	M DATA A56
SA_DQ57	AT40	M DATA A57	SA_DQ57	AT40	M DATA A57
SA_DQ58	AN38	M DATA A58	SA_DQ58	AN38	M DATA A58
SA_DQ59	AN39	M DATA A59	SA_DQ59	AN39	M DATA A59
SA_DQ60	AU38	M DATA A60	SA_DQ60	AU38	M DATA A60
SA_DQ61	AU39	M DATA A61	SA_DQ61	AU39	M DATA A61
SA_DQ62	AP39	M DATA A62	SA_DQ62	AP39	M DATA A62
SA_DQ63	AP40	M DATA A63	SA_DQ63	AP40	M DATA A63

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LGA1156

CPU-2

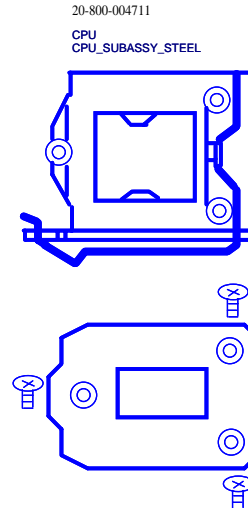
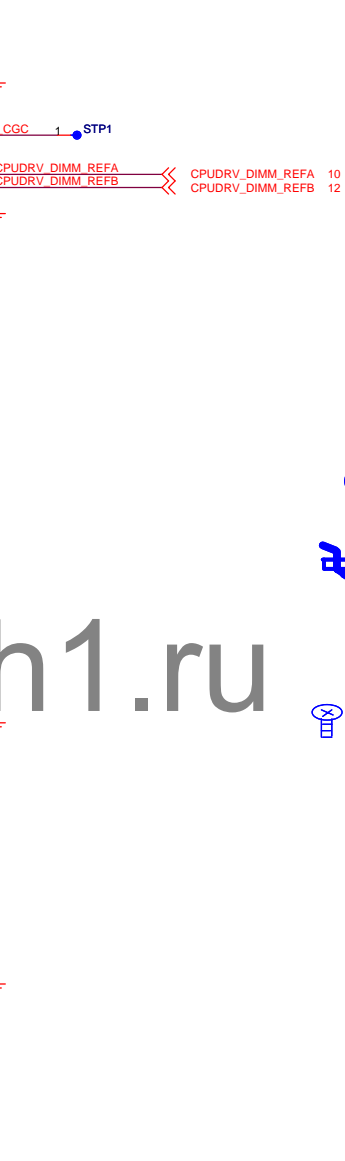
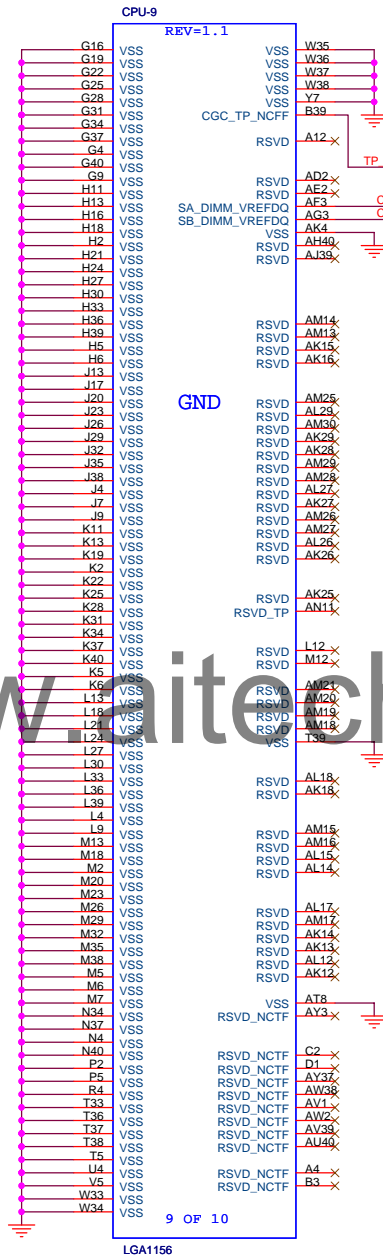
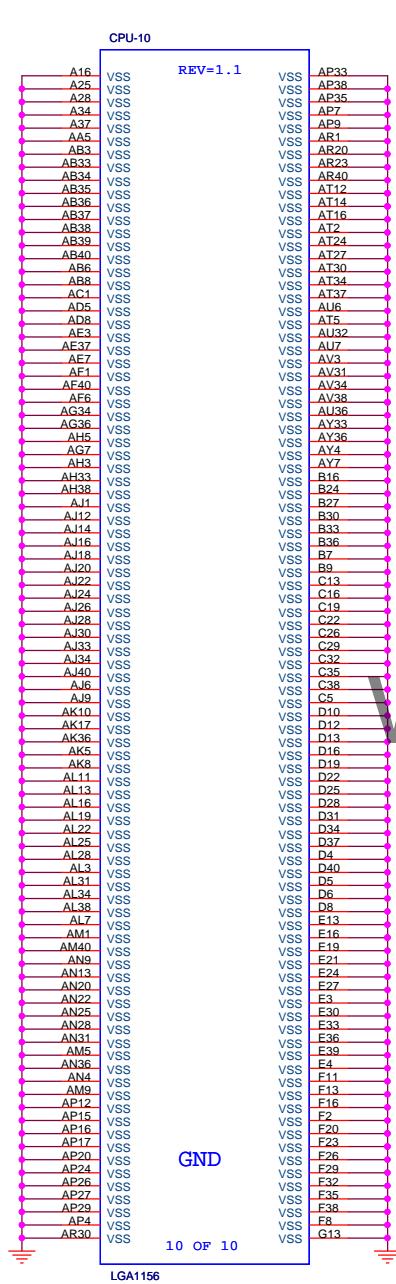
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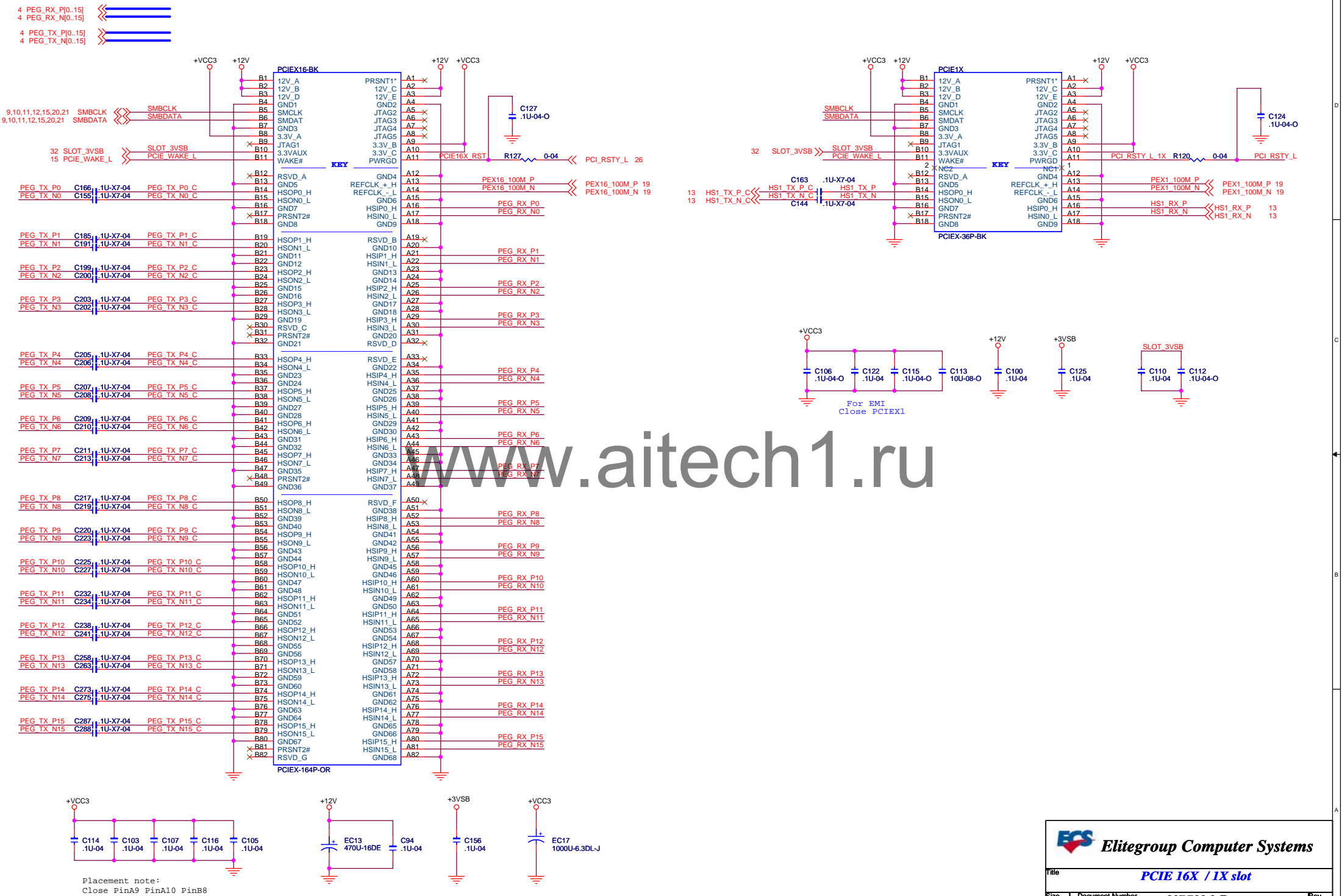
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M MAA B1	AU18	SB_MA[1]	SB_DQ5[0]	AE5	M DQS B DN0
M MAA B2	AV18	SB_MA[2]	SB_DM[0]	AE4	M DQM B0
M MAA B3	AU17	SB_MA[3]	SB_D00	AD7	M DATA B0
M MAA B4	AY18	SB_MA[4]	SB_D01	AD6	M DATA B1
M MAA B5	AW17	SB_MA[5]	SB_D02	AH8	M DATA B2
M MAA B6	AW16	SB_MA[6]	SB_D03	AJ8	M DATA B3
M MAA B7	AY16	SB_MA[7]	SB_D04	AC7	M DATA B4
M MAA B8	AY16	SB_MA[8]	SB_D05	AC5	M DATA B5
M MAA B9	AY25	SB_MA[9]	SB_D06	AF5	M DATA B6
M MAA B10	AW16	SB_MA[10]	SB_D07	AE6	M DATA B7
M MAA B11	AW15	SB_MA[11]	SB_DQ51	AH6	M DQS B DP1
M MAA B12	AY22	SB_MA[12]	SB_DQ51#0	AJ5	M DQS B DN1
M MAA B13	AW28	SB_MA[13]	SB_DM1	AH4	M DQM B1
M MAA B14	AY11	SB_MA[14]	SB_D08	AG5	M DATA B8
M MAA B15	AW27	SB_WE#	SB_D09	AH7	M DATA B9
M WE B L	AU26	SB_CAS#	SB_DQ10	AK6	M DATA B10
M CAS B L	AW27	SB_CAS#	SB_DQ11	AG6	M DATA B12
M_RAS B L	AW26	SB_RAS#	SB_DQ12	AG4	M DATA B13
M SBS B0	AU25	SB_BS[0]	SB_DQ13	AJ7	M DATA B14
M SBS B1	AW25	SB_BS[1]	SB_DQ14	AK7	M DATA B15
M SBS B2	AV12	SB_BS[2]	SB_DQ15	AK7	M DATA B15
M SCS B N0	AY27	SB_CS#0	SB_DQ52	AN6	M DQS B DP2
M SCS B N1	AW29	SB_CS#1	SB_DQ52#0	AM6	M DQS B DN2
M SCS B N2	AY26	SB_CS#2	SB_DM2	AM7	M DQM B2
M SCS B N3	AY29	SB_CS#3	SB_DQ16	AL6	M DATA B16
M SCKE B0	AW8	SB_CKE[0]	SB_DQ17	AN6	M DATA B17
M SCKE B1	AU8	SB_CKE[1]	SB_DQ18	AP6	M DATA B18
M SCKE B2	AV8	SB_CKE[2]	SB_DQ19	AR5	M DATA B19
M SCKE B3	AV9	SB_CKE[3]	SB_DQ20	AL5	M DATA B20
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M ODT B1	AU28	SB_ODT[1]	SB_DQ22	AN7	M DATA B22
M ODT B2	AV27	SB_ODT[2]	SB_DQ23	AP5	M DATA B23
M ODT B3	AU28	SB_ODT[3]	SB_DQ53	AR8	M DQS B DP3
CK M DDR0 B DP	AR17	SB_CK[0]	SB_DQ53#0	AP8	M DQS B DN3
CK M DDR0 B DN	AR16	SB_CK[0]	SB_DM3	AT7	M DQM B3
CK M DDR1 B DP	AT15	SB_CK[1]	SB_DQ24	AT6	M DATA B24
CK M DDR1 B DN	AN15	SB_CK[1]	SB_DQ25	AR7	M DATA B25
CK M DDR2 B DP	AN17	SB_CK[2]	SB_DQ26	AR9	M DATA B26
CK M DDR2 B DN	AN17	SB_CK[2]	SB_DQ27	AM8	M DATA B27
CK M DDR3 B DP	AN16	SB_CK[3]	SB_DQ28	AN8	M DATA B28
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ29	AR6	M DATA B29
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ30	AL8	M DATA B30
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ31	AT9	M DATA B31
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ32	AT25	M DQS B DP4
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ33	AR24	M DQS B DN4
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DM4	AN24	M DQM B4
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ34	AN23	M DATA B32
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ35	AP23	M DATA B33
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ36	AR25	M DATA B34
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ37	AR26	M DATA B35
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ38	AT23	M DATA B36
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ39	AP22	M DATA B37
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ40	AP25	M DATA B38
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ41	AT26	M DATA B39
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ42	AP32	M DQS B DP5
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ43	AR32	M DQS B DN5
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ44	AN32	M DQM B5
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ45	AT32	M DATA B40
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ46	AP31	M DATA B41
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ47	AR33	M DATA B42
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ48	AM32	M DATA B43
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ49	AT31	M DATA B44
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ50	AR31	M DATA B45
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ51	AR34	M DATA B46
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ52	AT33	M DATA B47
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ53	AR36	M DQS B DP6
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ54	AR37	M DQS B DN6
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ55	AM33	M DQM B6
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ56	AR35	M DATA B48
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ57	AT36	M DATA B49
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ58	AN33	M DATA B50
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ59	AP36	M DATA B51
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ60	AP34	M DATA B52
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ61	AT35	M DATA B53
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ62	AN34	M DATA B54
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ63	AP37	M DATA B55
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ64	AL37	M DQS B DP7
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ65	AM36	M DQS B DN7
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ66	AK35	M DQM B7
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ67	AL35	M DATA B56
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ68	AM35	M DATA B57
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ69	AJ36	M DATA B58
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ70	AJ37	M DATA B59
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ71	AN35	M DATA B60
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ72	AM34	M DATA B61
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ73	AJ35	M DATA B62
CK M DDR3 B DN	AR18	SB_CK[3]	SB_DQ74	AL36	M DATA B63

DDR_B

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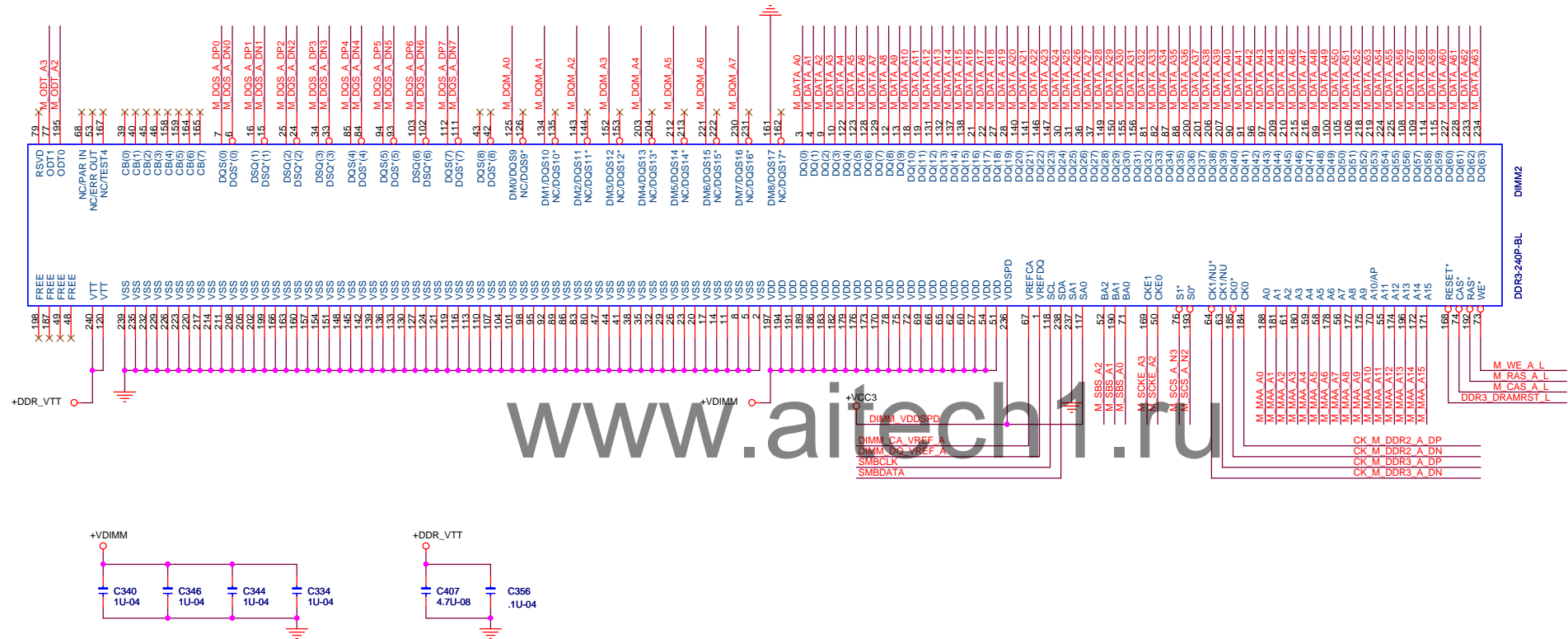
LGA1156



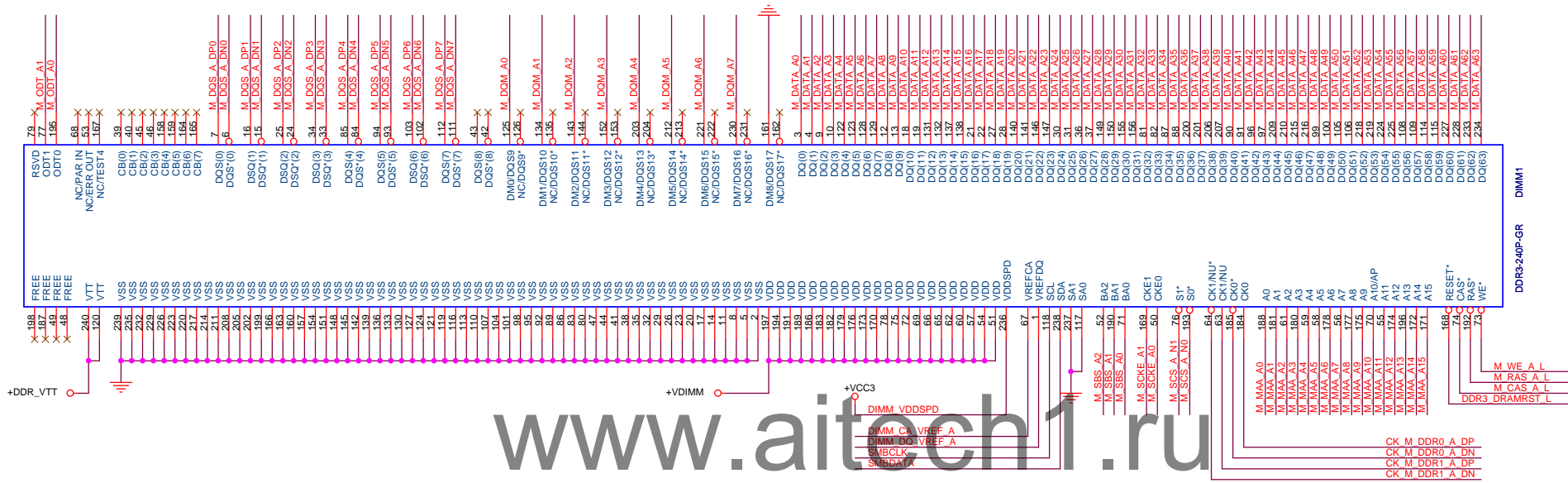


Placement note:
Close PinA9 PinA10 PinB8

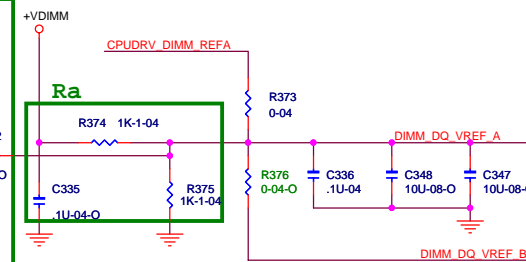
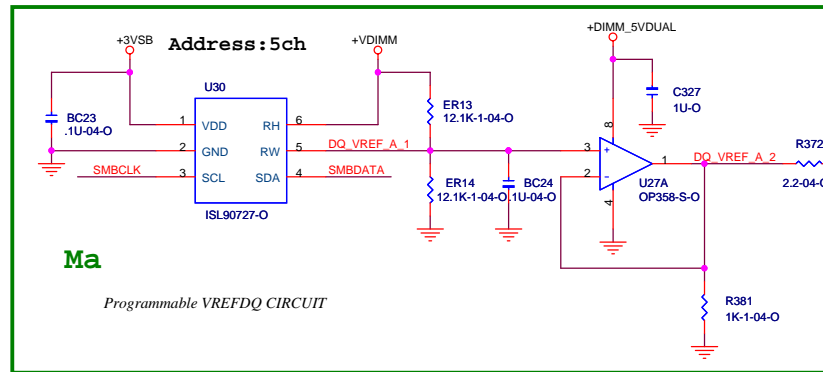
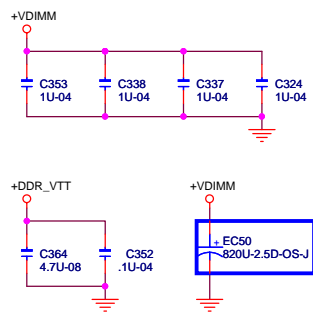
CHANNEL A DIMM1



CHANNEL A DIMM0

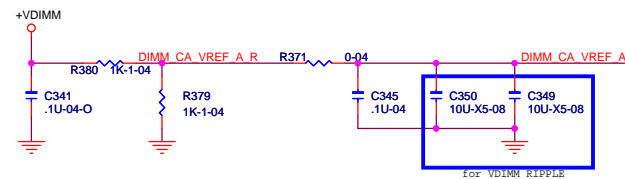


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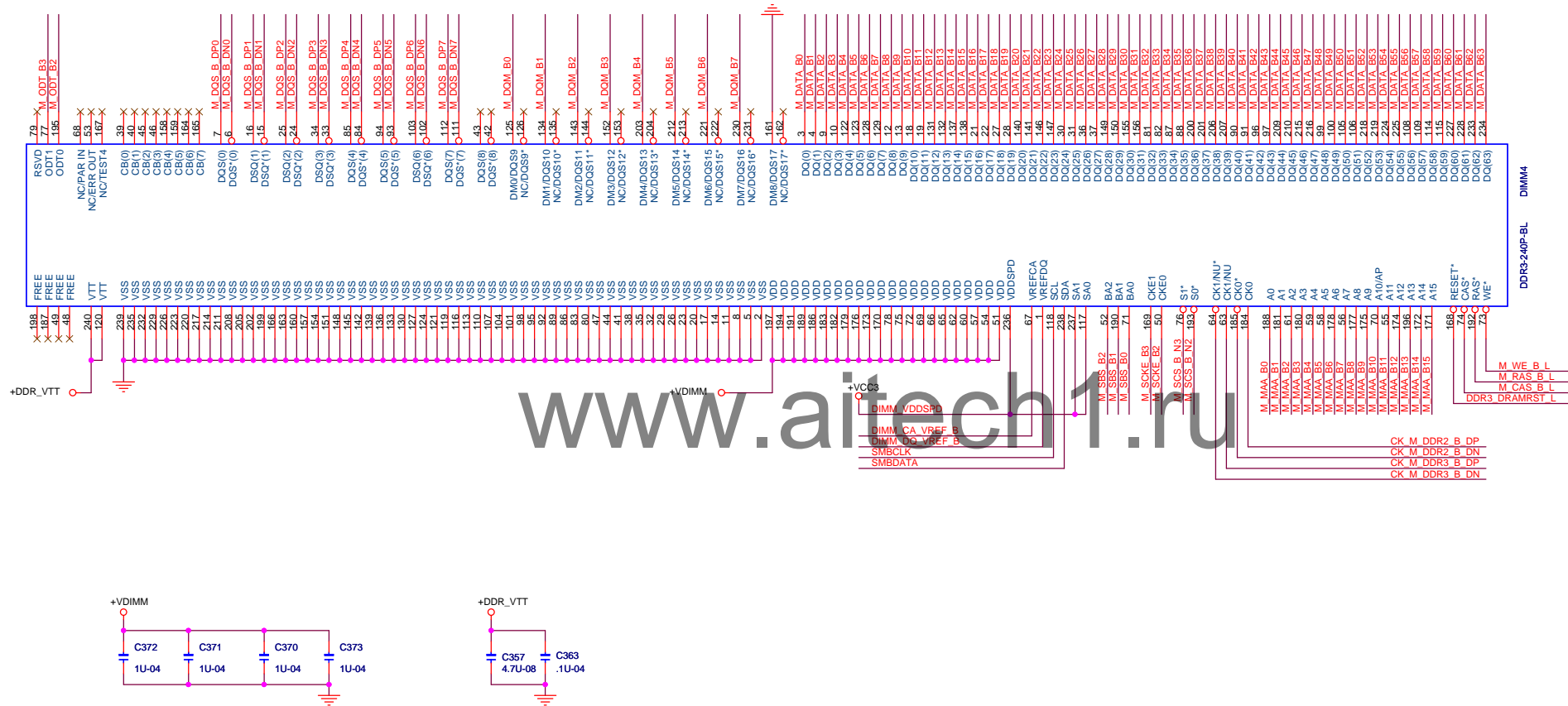


DQ_VREF Control Mode

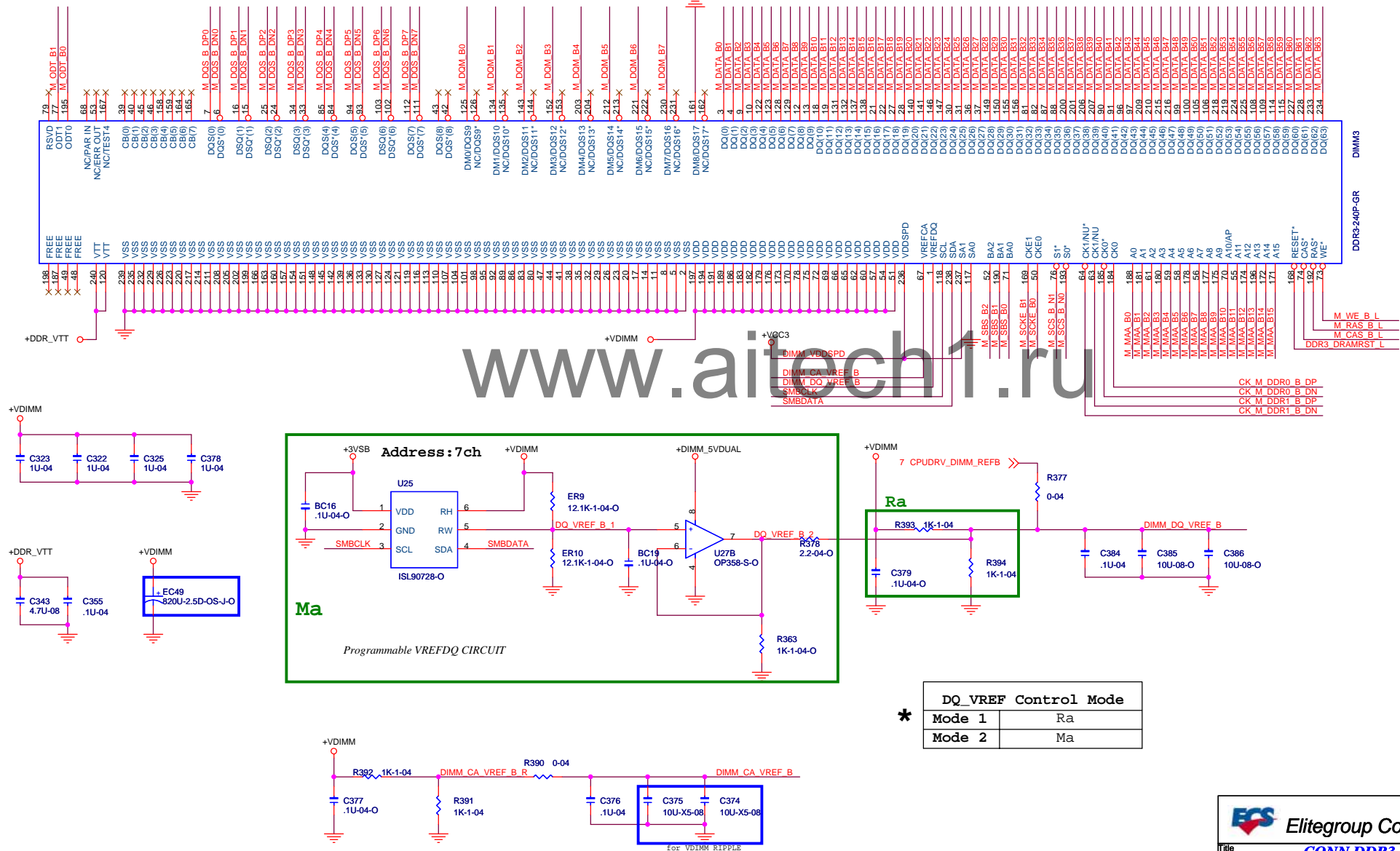
Mode 1	Ra
Mode 2	Ma



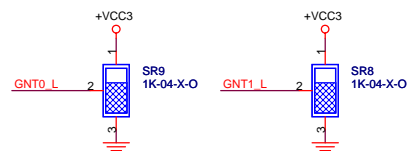
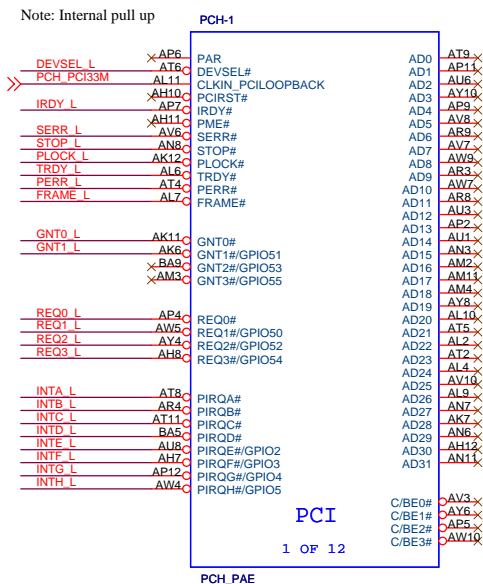
CHANNEL B DIMM1



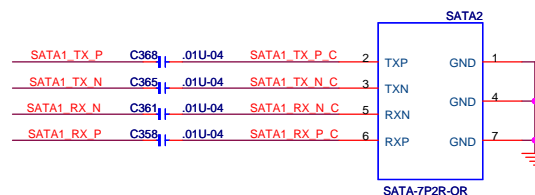
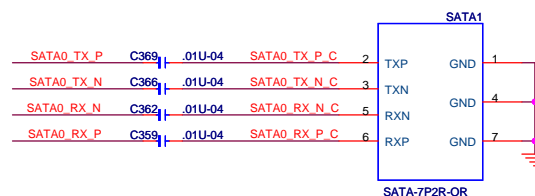
CHANNEL B DIMM0

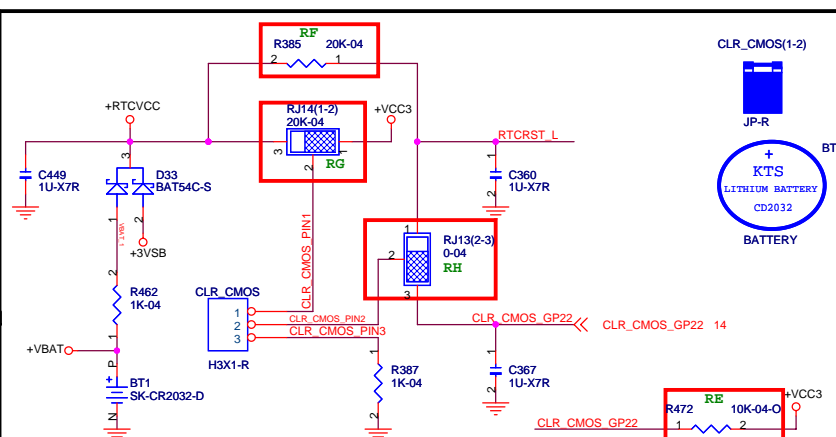
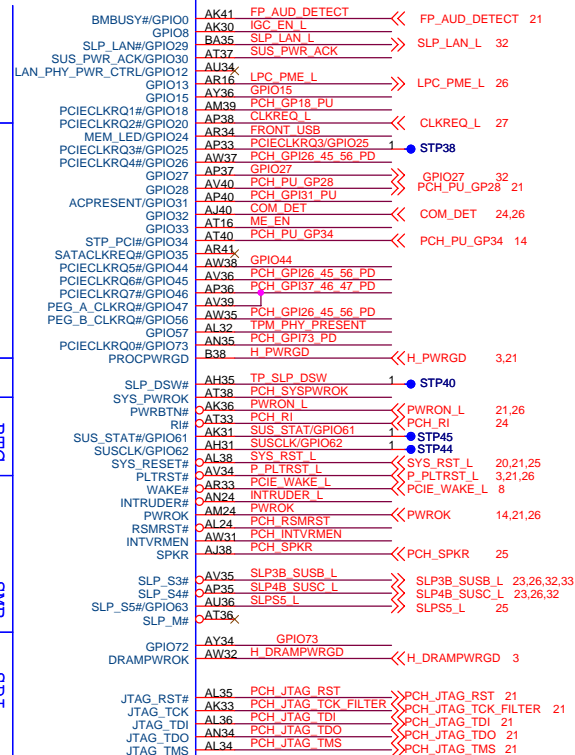
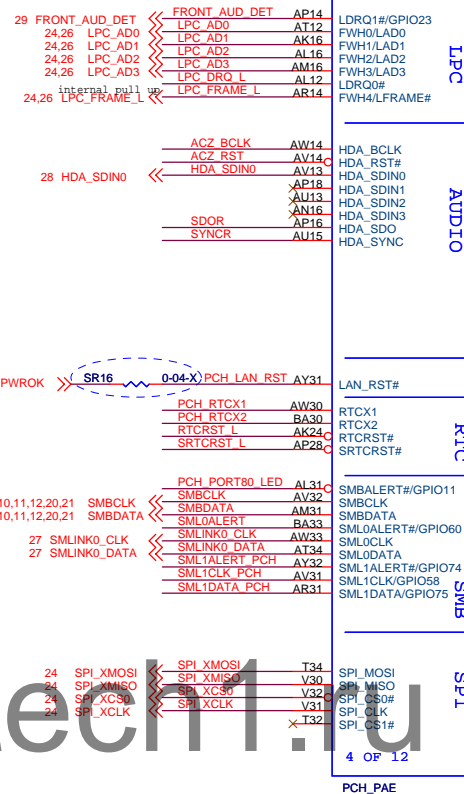
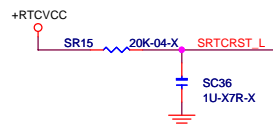
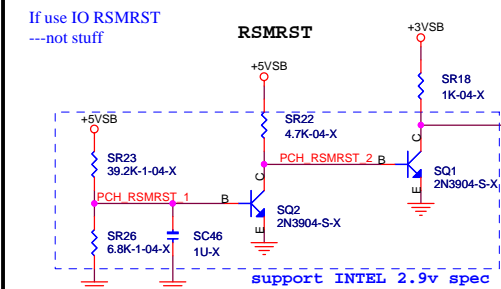
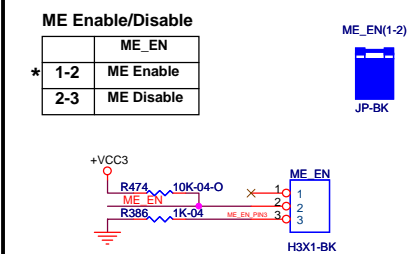
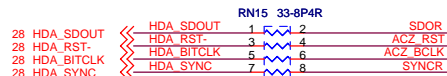
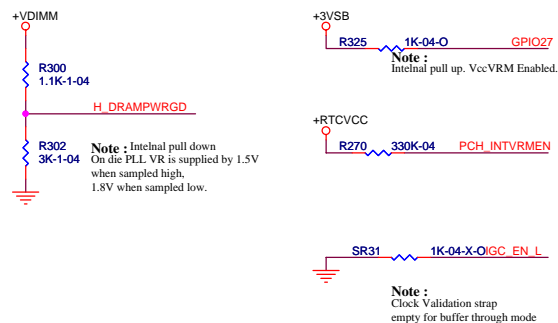


✱	DQ_VREF Control Mode	
	Mode 1	Ra
	Mode 2	Ma



BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1





CLR_CMOS				
1-2	NORMAL			
2-3	CLEAR CMOS			

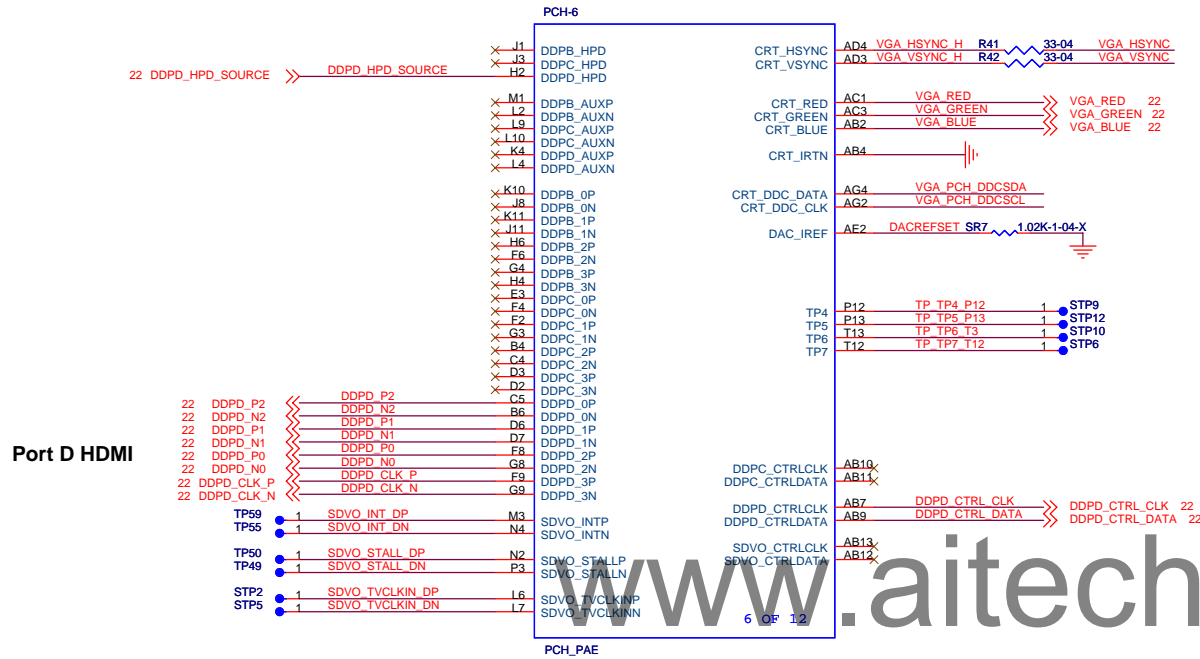
	RE	RF	RG	RH
*S/W	NC	20K	(1-2)	(2-3)
H/W	10K	NC	(2-3)	(1-2)

Note :

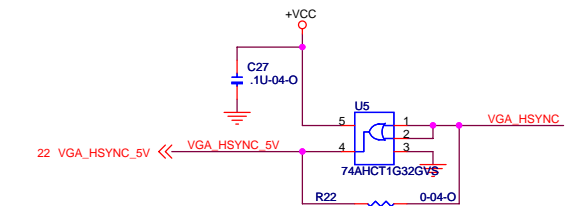
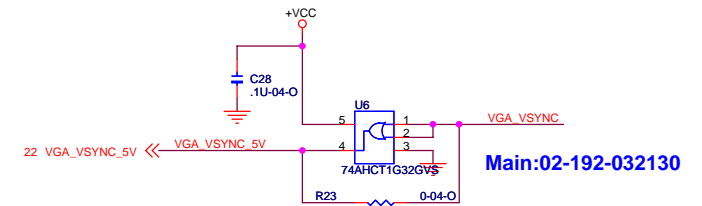
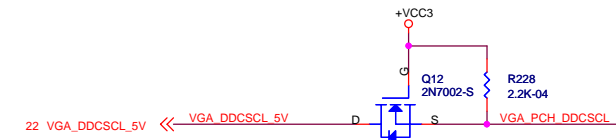
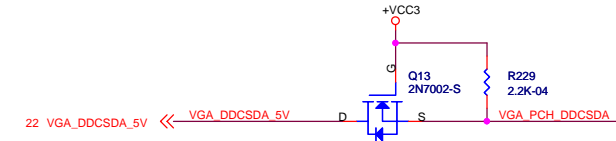
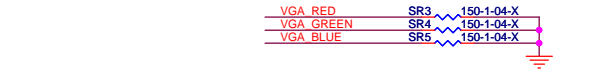
Port B:Capable of SDVO/HDMI/DVI/DP

Port C:Capable of HDMI/DVI/DP

Port D:Capable of HDMI/DVI/DP



Port	Strap	How to enable the port	How to Disable the Port
Port B	SDVO_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC
Port C	DDPC_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC
Port D	DDPD_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC



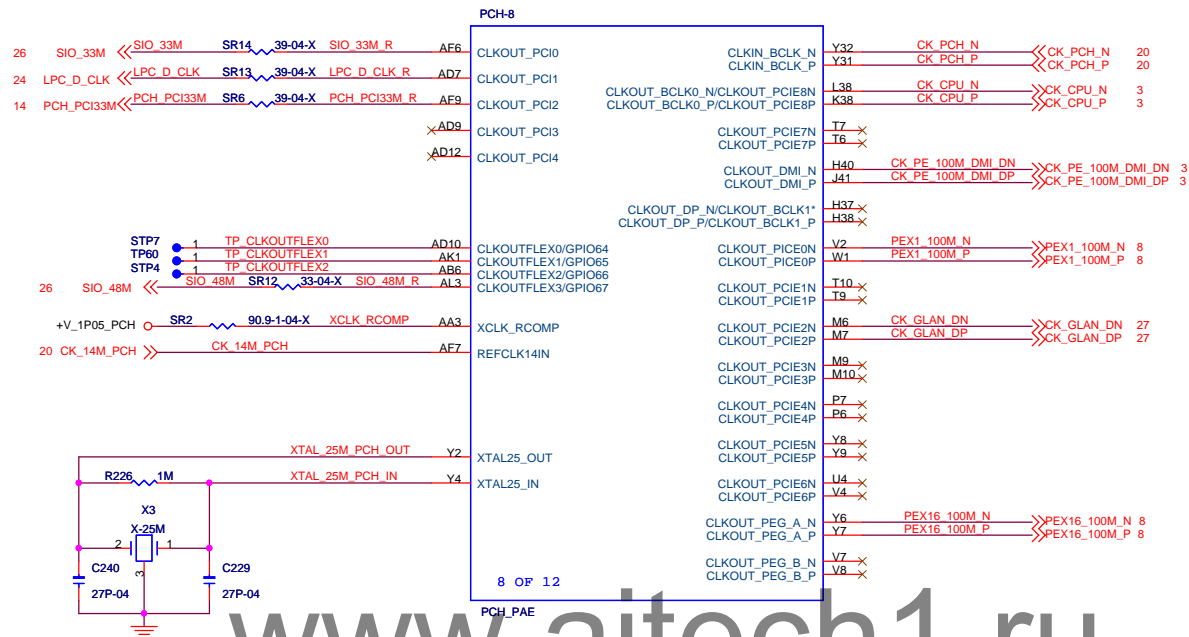
SC8 10P-04-X PCH PCI33M R

SC29 10P-04-X SIO_33M R

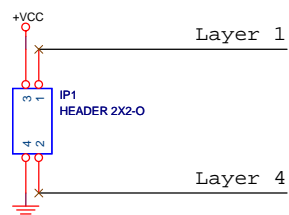
SC23 22P-04-X-O SIO_48M R

SC30 10P-04-X-O LPC_D_CLK R

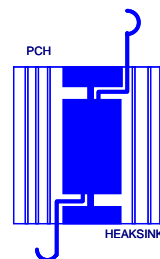
C245 10P-04-O CK_14M PCH



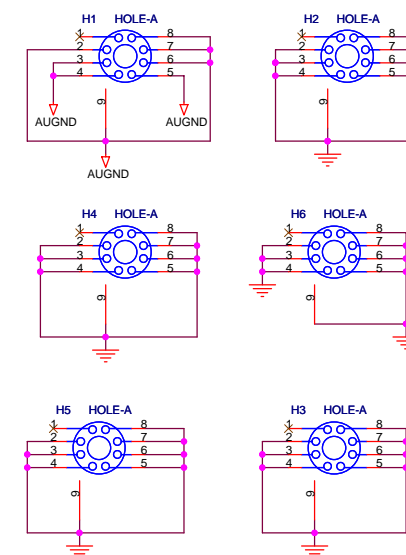
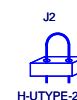
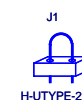
PCIE(16X)

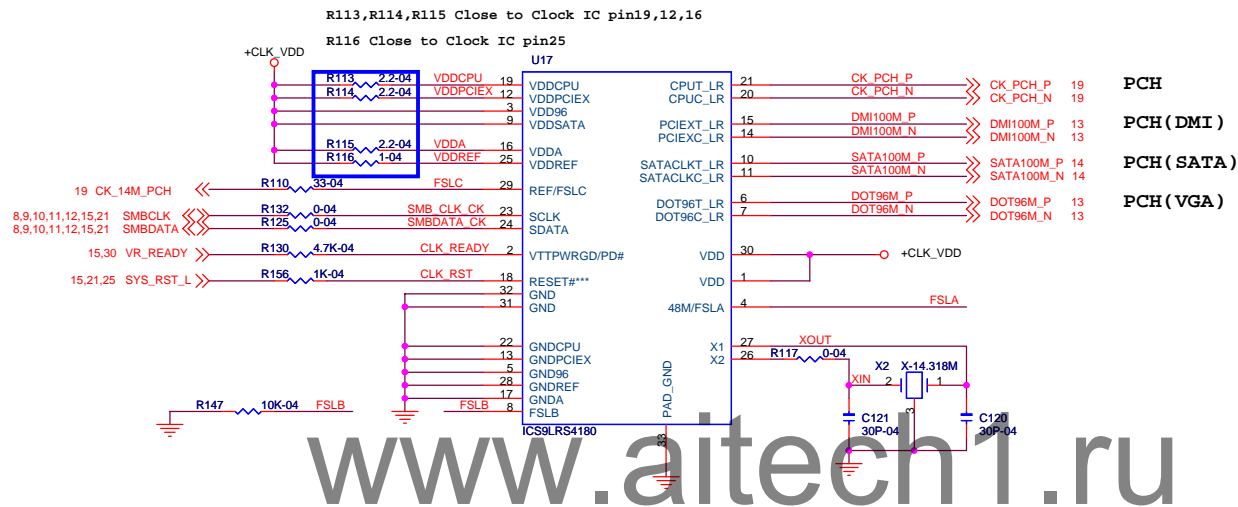


```
1080 : trace width 4 mil 50 ohm
      Trace Length 3150 mils
      Spacing: 1.clearance to itself 50/4/50(S:W:S)
               2.clearance to other signal 3W
```



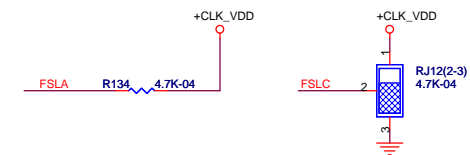
Main:add new P/N



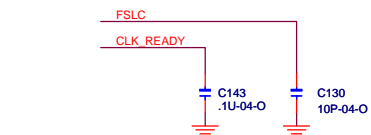
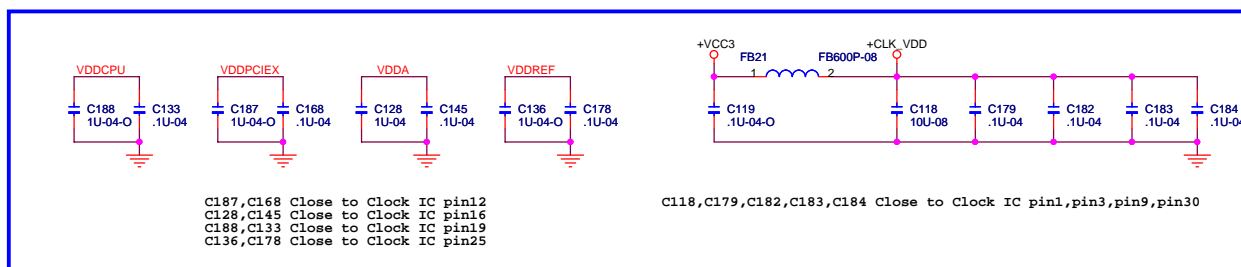


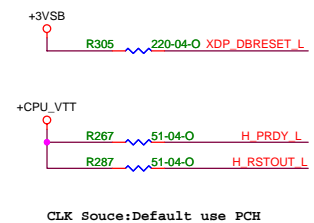
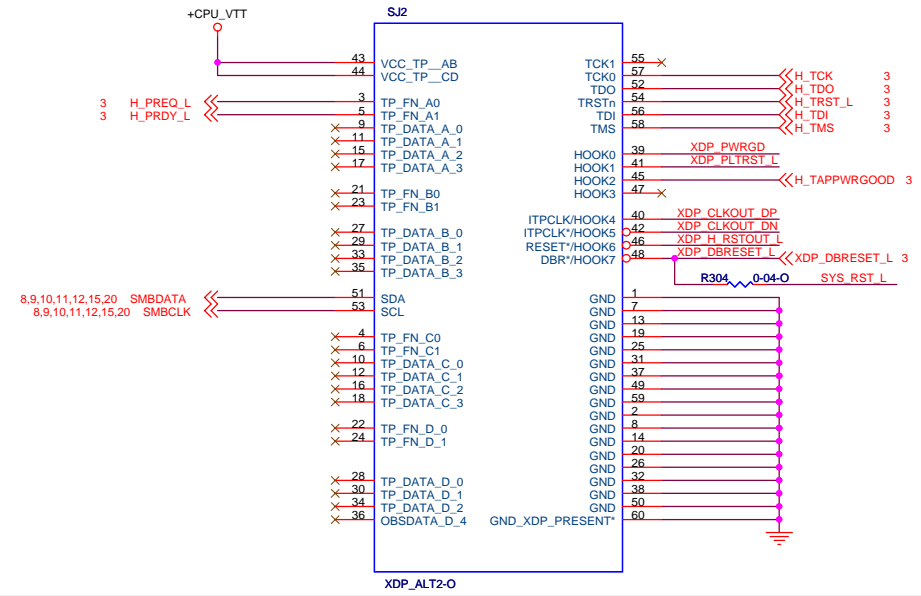
CPU CLK Table

FSLA	FSLC	CPU CLK(MHz)
1	0	133
1	1	100

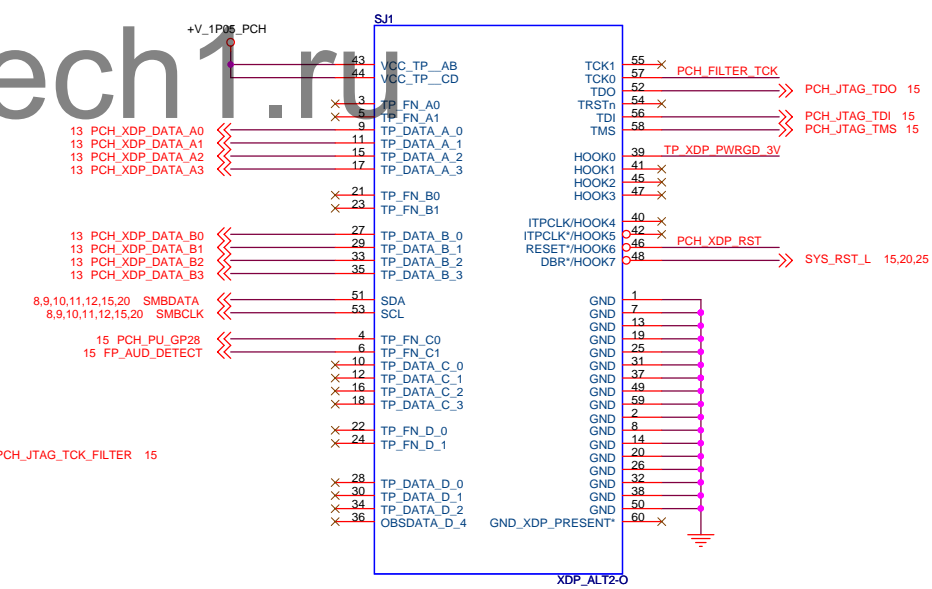


12/1 IDT had suggestions schematic with update 9LPRS4180





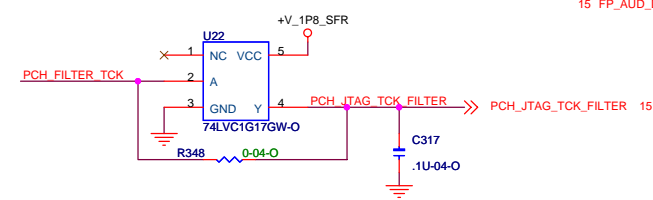
CLK Souce:Default use PCH



```


DESIGN NOTE:
DEFAULT EMPTY SITE ON PAGE 94: XDP_PWRGD RES (R108PR) TO VTT_OUT_RIGHT
DEFAULT EMPTY SITE ON PAGE 123: XDP_PWRGD RES (R3S3EV) TO V_FSB_VTT
DEFAULT STUFF SITE: (R662EV) TO TP_XDP_PWRGD

```

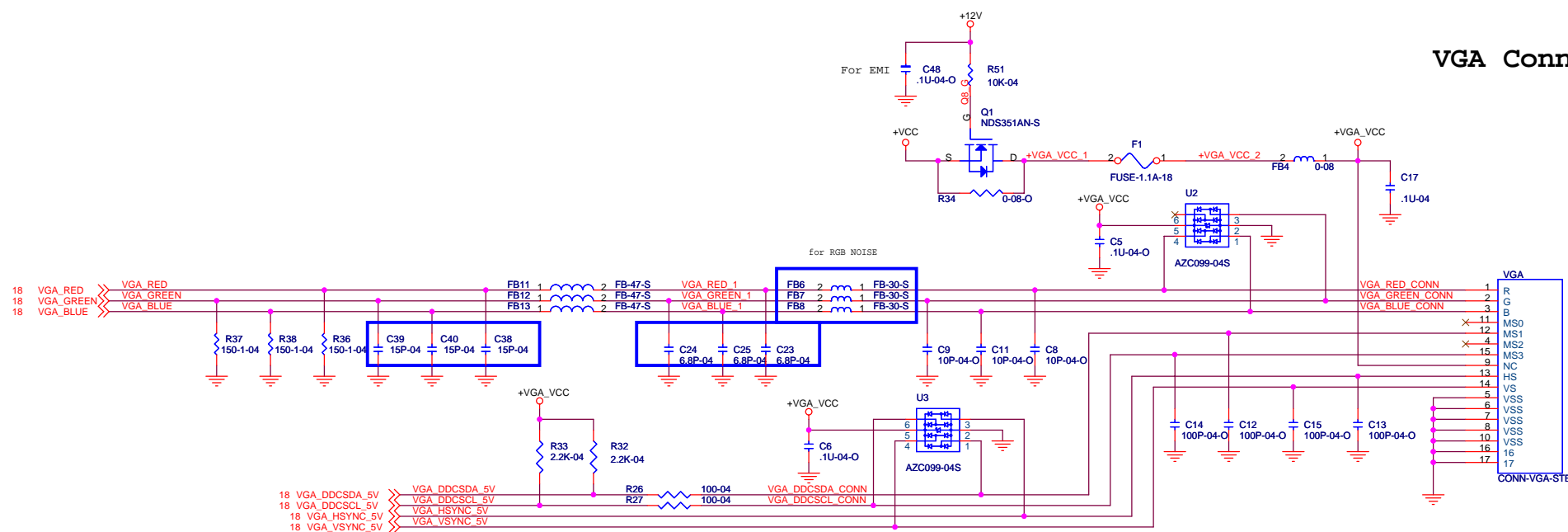


PCH PIN	ES1	ES2	Production Systems
TD0	No Stuff	100 Ohms	51 Ohms
TMS	100 Ohms	100 Ohms	51 Ohms
TDI	100 Ohms	100 Ohms	51 Ohms
TRST#	10K Ohms	10K Ohms	51 Ohms
RJ24	0(2-3)	0(2-3)	0(1-2)

DESIGN NOTE: PCH JTAG

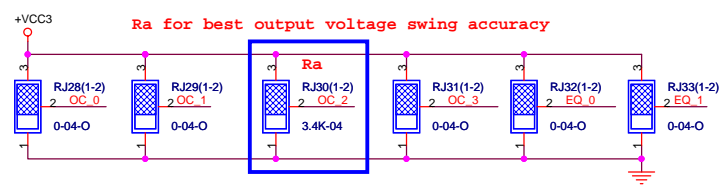
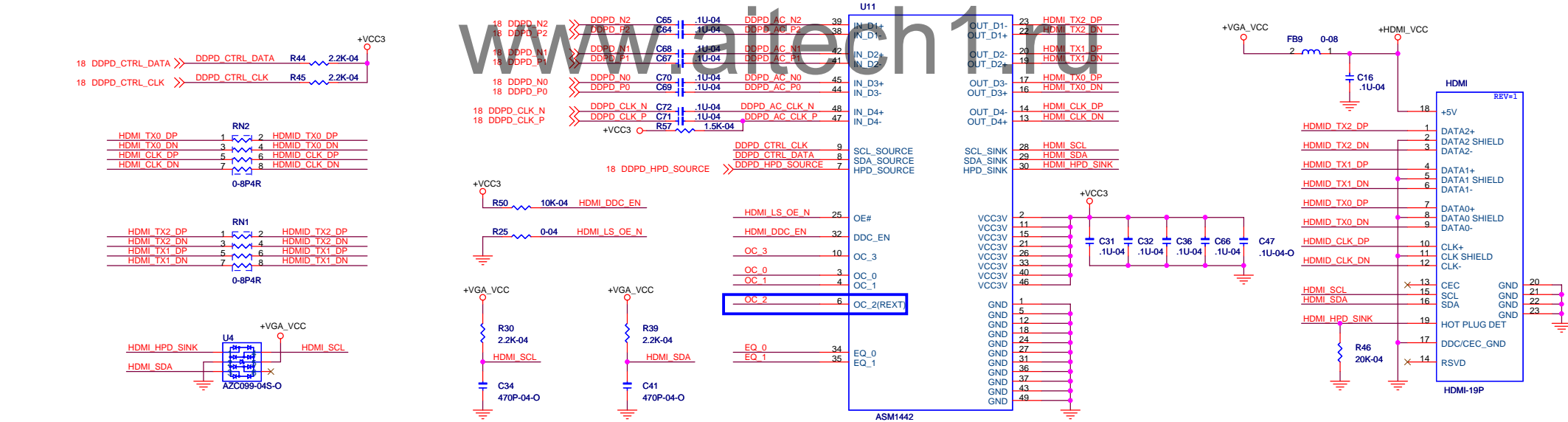
 <h1 style="margin: 0;">Elitegroup Computer Systems</h1>					
Title					
<i>Primary&PCH XDP</i>					
Size	Document Number				Rev
Custom	H55H-LD				1.0
Date:	Monday, February 01, 2010			Sheet	21 of 37

VGA Connector



Level Shifter

HDMI Connector



For Ibex-Peak Platform --- non-inverting

Asmedia : 02-342-442070 IC SWITCH.ASM1442..QFN48P.LEAD-FREE(RoHS).ASMT
NXP : 02-342-360121 IC SWITCH.PTN3360BBS..HVQFN48P.LEAD-FREE.NXP

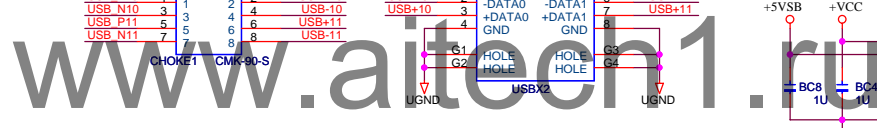
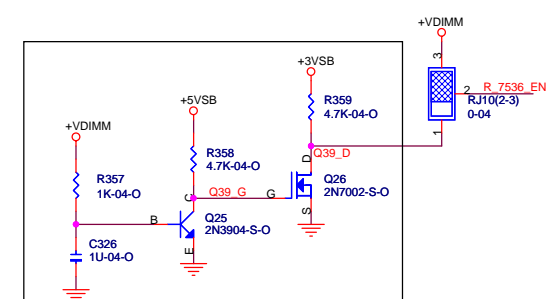
For Eagle-Lake Platform--- inverting

Asmedia : 02-342-442071 IC SWITCH.ASM1442T..QFN 48P.LEAD-FREE(RoHS).ASMT
NXP : 02-342-360120 IC SWITCH.PTN3360ABS..HVQFN 48P.LEAD-FREE.NXP

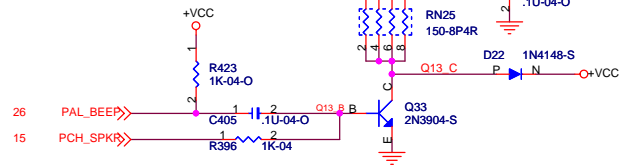
Elitegroup Computer Systems

VGA&DMI Level Shifter

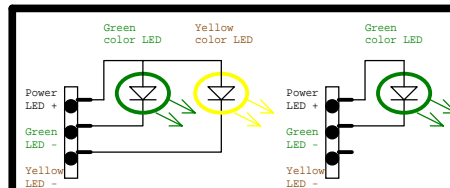
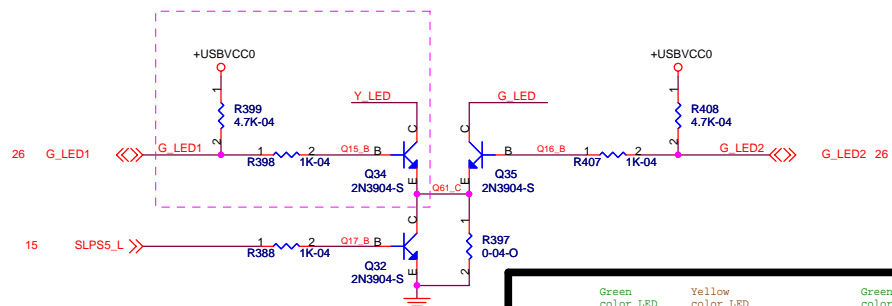
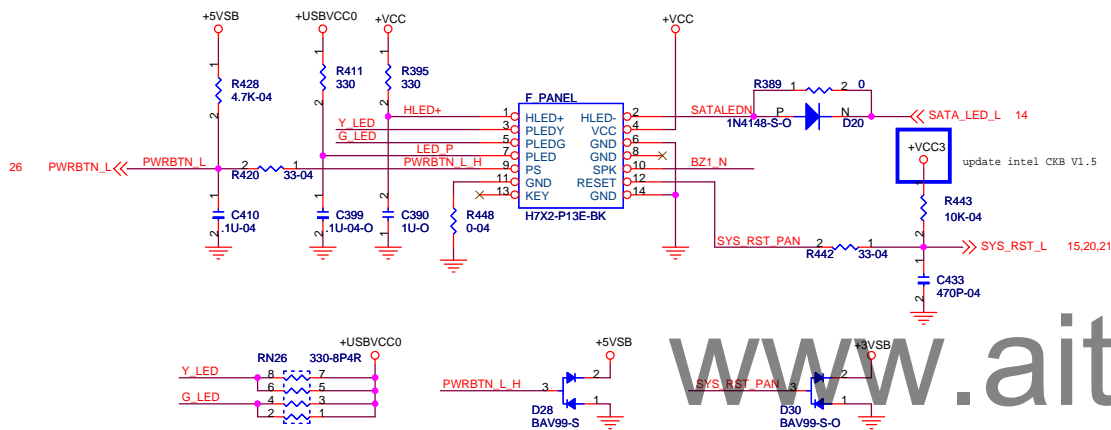
File	H55H-LD		Rev	1.0
Size	Document Number			
Custom				
Date	Monday, February 01, 2010	Sheet	22	of 37

[illegible]

BUZZER



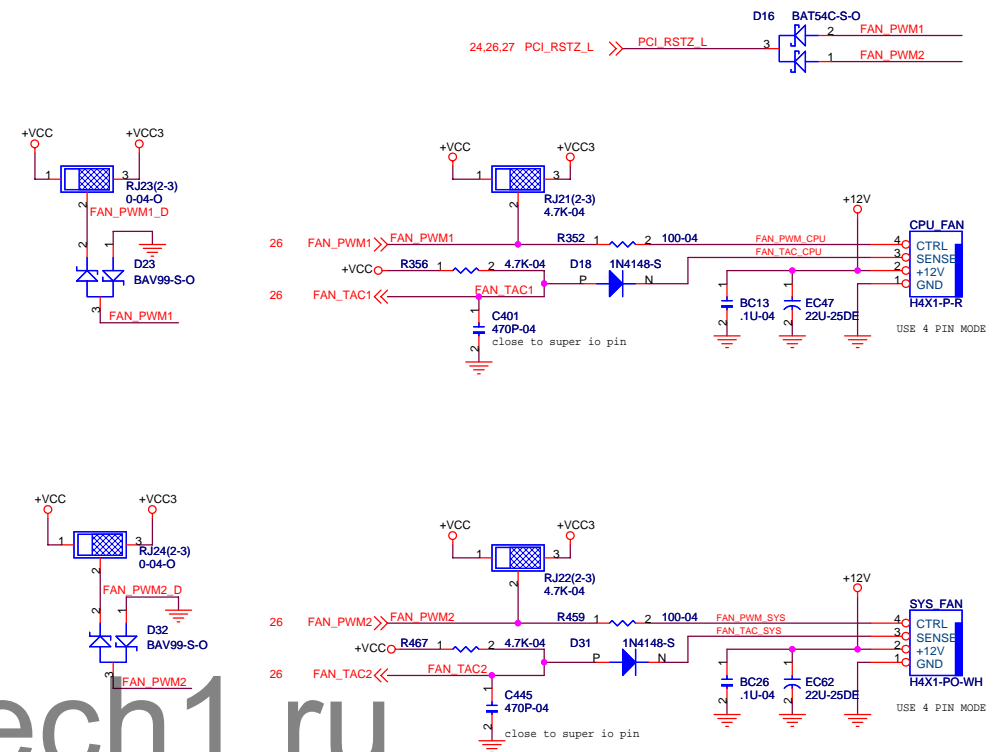
F_PANEL



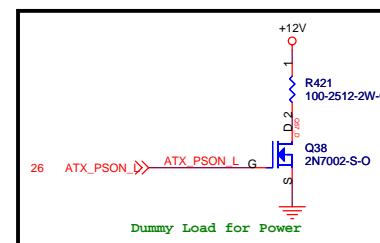
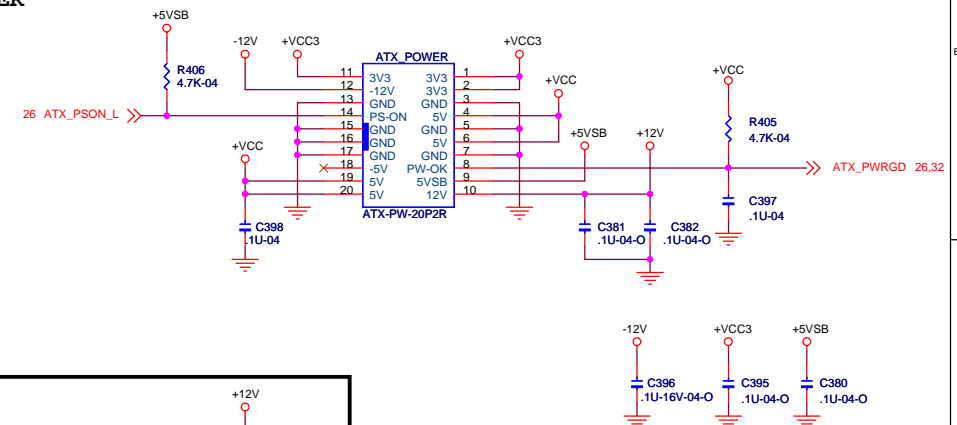
3-Pin dual color LED	
S0	Steady Green
S1	Green Blinking (Frequency: 1Hz)
S3	Steady Yellow
S4/S5	OFF

2-Pin single color LED	
S0	Steady Green
S1/S3	Green Blinking (Frequency: 1Hz)
S4/S5	OFF

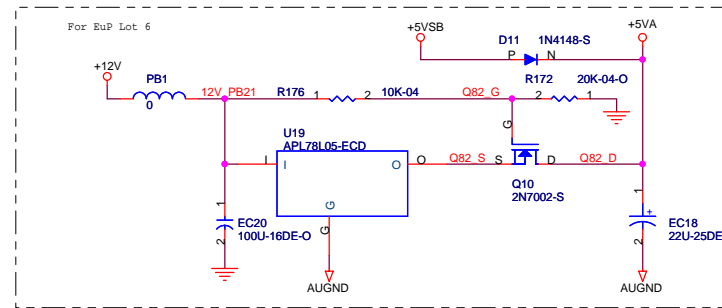
FAN CONTROL



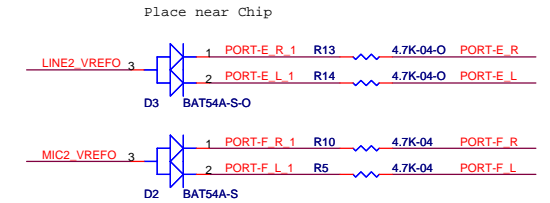
ATXPOWER



```
1.Pin 52:VIN3/ATXPG
2.Pin 32:SUSB#
3.Pin 25/ Pin 58/ Pin 60/ Pin 62
4.Pin 10:RESETCON#
```

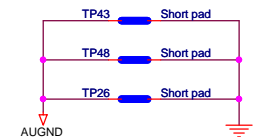
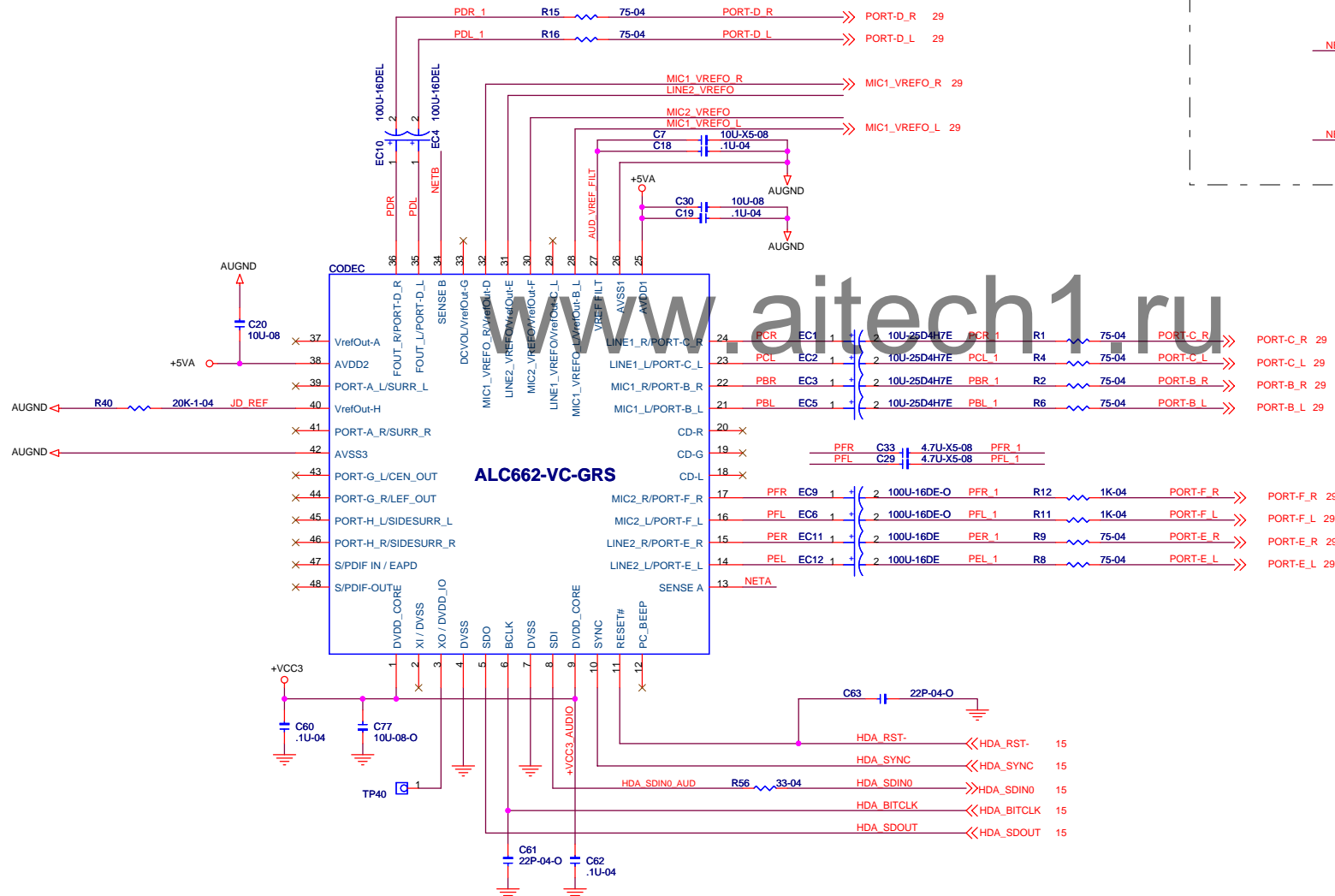
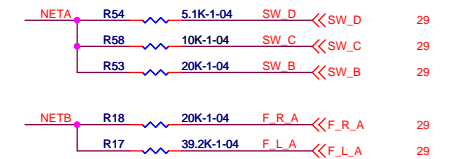



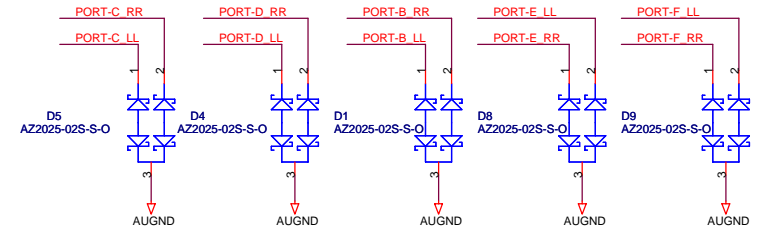
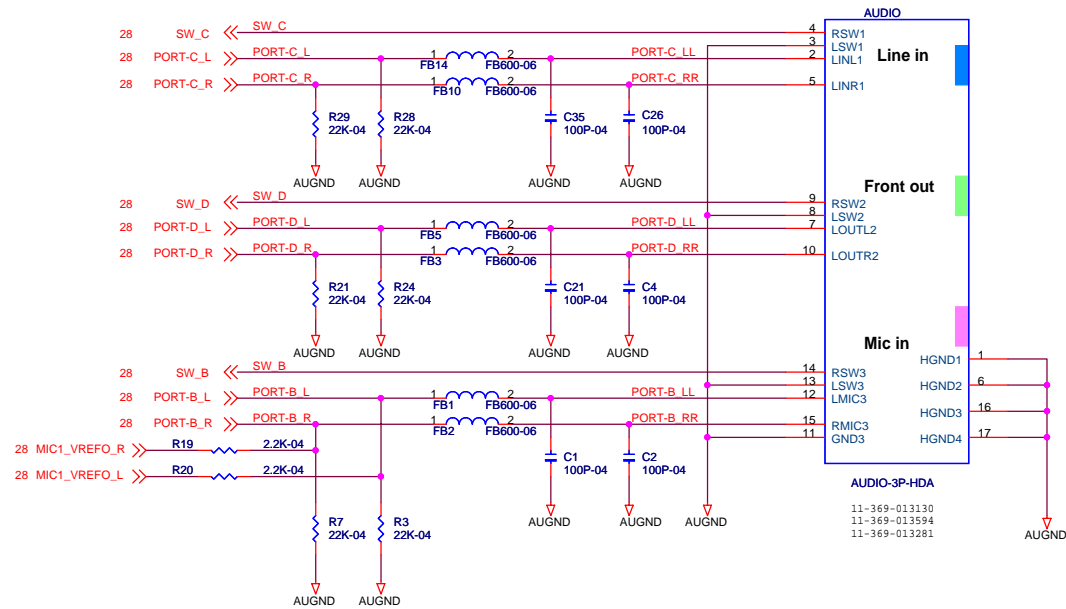
Verfourt bias for stereo microphone.



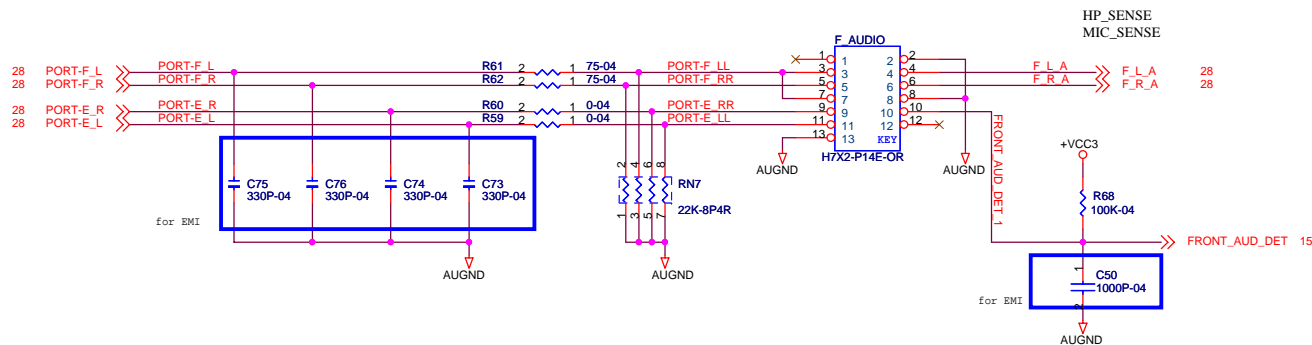
Resistors Networks

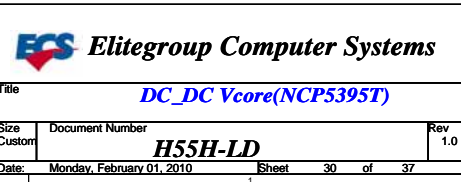
Place near Chip

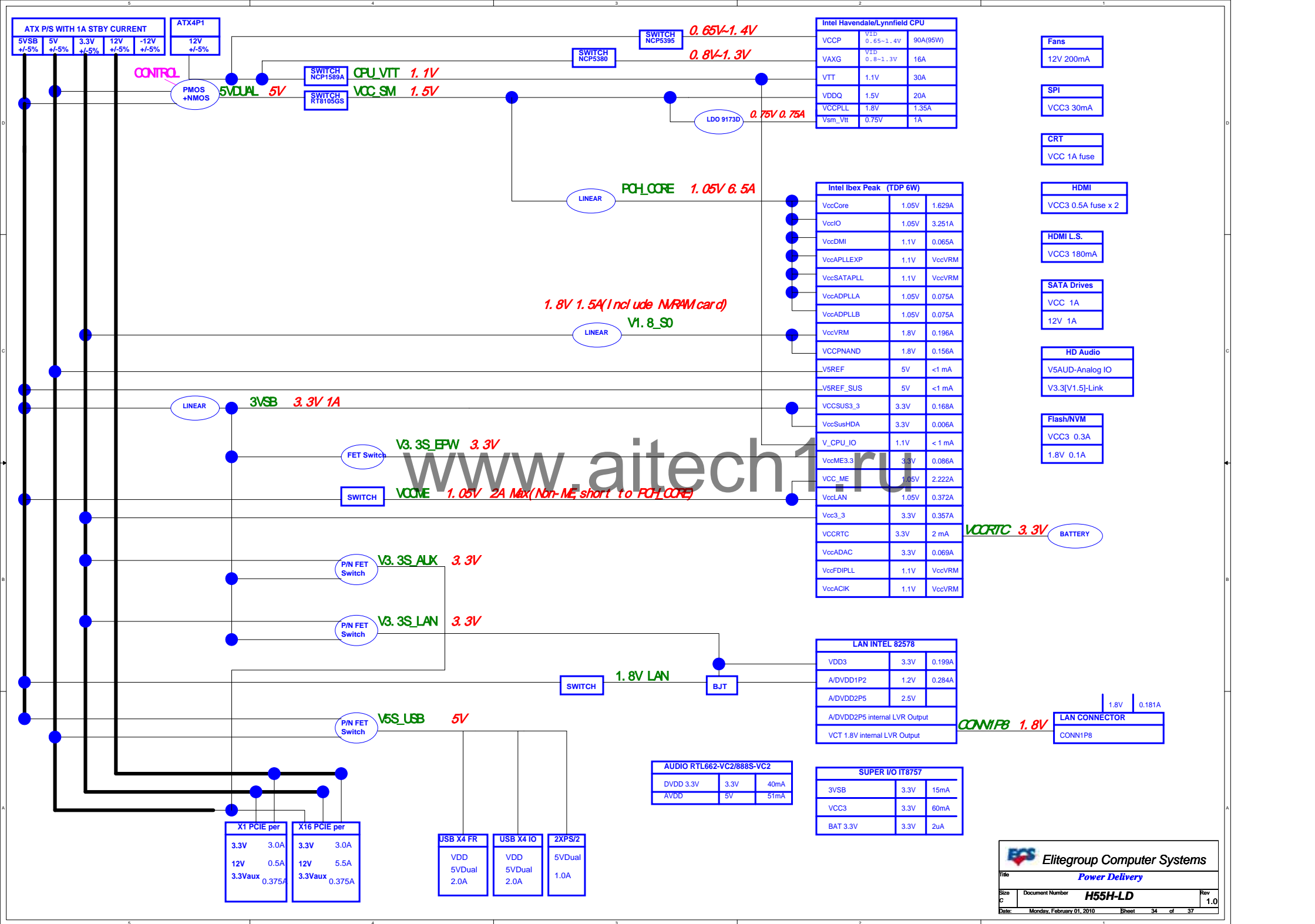


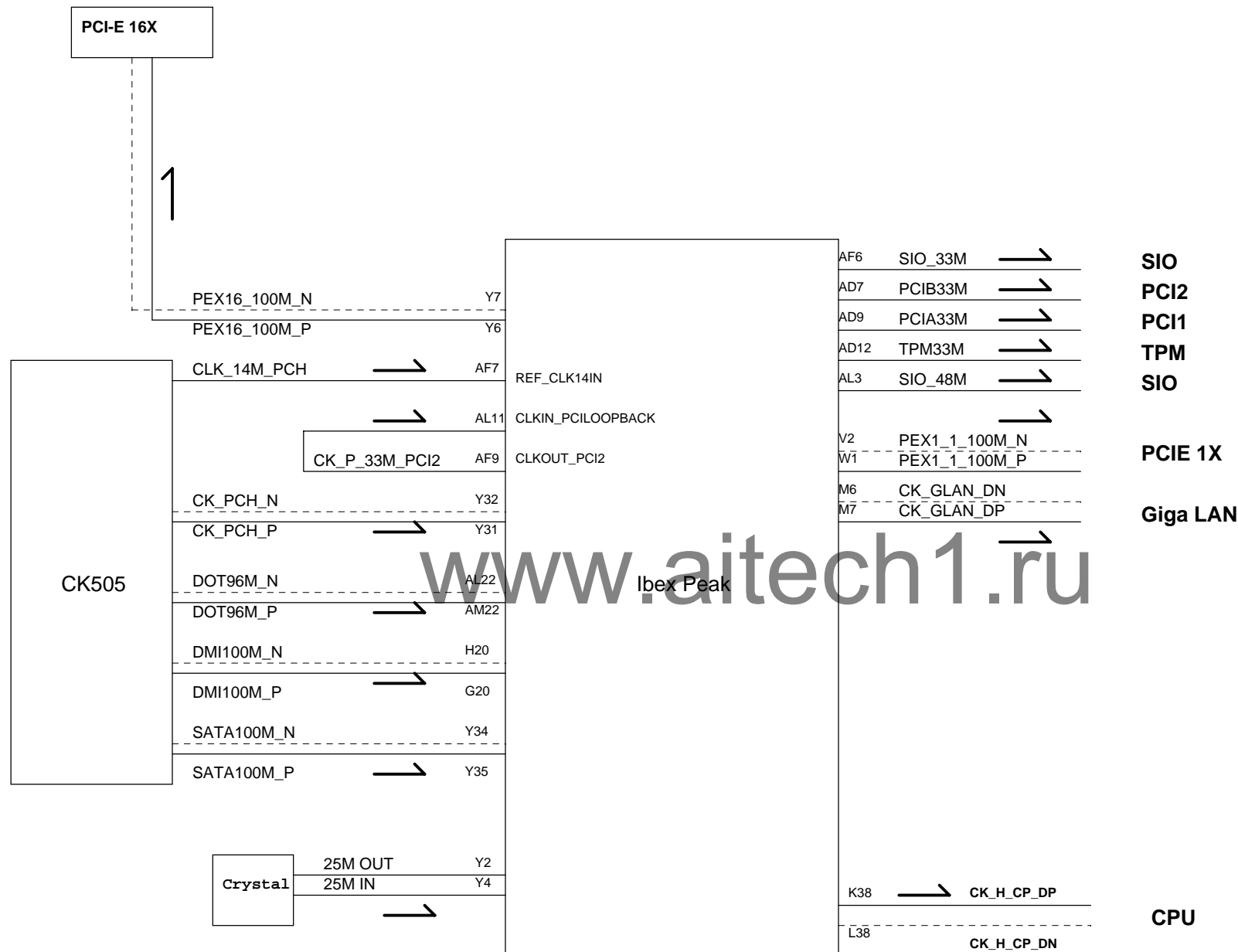


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CPU Strap Function

CFG	Havendale	Lynnfield			
0	REVERSED	1	11=1*16X	0	10=2*8X
1	REVERSED	1		1	
2	REVERSED			REVERSED	
3	Static Lane Number Reversal			REVERSED	
4	REVERSED			REVERSED	
6	REVERSED				
7	REVERSED				
15	REVERSED				
0,1,2,3,4,5 ALL HAVE INTERNAL PULL-UPS					

POWER ON CONFIGURATION (POC)TABLE

	FUNCTION	Setting	Clarkdale	Lynnfield
VID0	MIS0	1	Support (09A)	Support (09A)
VID1	MIS1	0		
VID2	MIS2	1		
VID3	IMON CONFIG0	1	Icc(MAX)=120A	Icc(MAX)=120A
VID4	IMON CONFIG1	0		
VID5	IMON CONFIG2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

Clock(ICS9LRS4180) Strap Function

Functionality Table FSLC,FSLA = 01, CPU_CLK = 133MHz

Bit2 FSLC	Bit1 FSLB	Bit0 FSLA	CPU MHZ	PCIEX MHZ	SATA MHZ	DOT96 MHZ
0	0	1	133.33	100.00	100.00	96.00
1	0	1	100.00	100.00	100.00	96.00

PCIEX PLL Spread Frequency Selection Table

B19b4	B19b3	FSLC B0b2	FSLB B0b1	FSLA B0b0	PCIEX	Spread
					MHZ	%
0	0	0	0	1	100.00	0.5% Down
0	0	1	0	1	100.00	0.5% Down
1	0	0	0	1	100.00	NO Spread
1	0	1	0	1	100.00	NO Spread

CPU PLL Spread Frequency Selection Table

FSLC B0b2	FSLB B0b1	FSLA B0b0	CPU MHZ	Spread% B0b5=1
0	0	1	133.33	0.5% Down
1	0	1	100.00	0.5% Down

PCH Strap Function


BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

IBEX GPIO Table

Name	Type	Voltage	Default	Functional Description	Function
GPIO0	I/O	+VCC3	GPI	BMBUSY	FP_AUD_DET
GPIO11	I/O	+3VSB	SMBALERT#	SMBALERT#	PCH_PORT80_LED
GPIO13	I/O	+3VSB	GPI	GPI13	LPC_PME_L
GPIO20	I/O	+VCC3	GPO	PCICLKQ2	CLKREQ_L
GPIO22	I/O	+VCC3	GPI	SCLOCK	CLR_COMS
GPIO23	I/O	+VCC3	GPO	BMBUSY	FRONT_AUD_DET
GPIO27	I/O	+3VSB	GPO	GPO27	Enable PCIE 3.3VSB
GPIO38	I/O	+VCC3	GPO	GPO38	COM_DET

ITE8757 GPIO Table

Name	Type	Voltage	Default	Functional Description	Function
GP25	DIOD8	VCCH	GPO25	GPIO25	Y LED CONTROL
GP26	DIOD8	VCCH	GPO26	GPIO26	G LED CONTROL
GP12	DIOD8	+VCC	PCI Reset 1#	PCI Reset 1# / GPIO 12	WT_BEEP
GP40	DIOD8	VCCH	3VSBSW#	3VSBSW# / GPIO 40	DIMM_5VDUAL CONTROL



Title

GPIO/STARP

Size Custom

Document Number

Rev 1.0

Date:

Monday, February 01, 2010

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